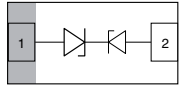


# Bidirectional Asymmetrical (BiAs) Single Line ESD Protection Diode in DFN1006-2A



20950


**MARKING** (example only)


Bar = pin 1 marking  
 Y = type code (see table below)  
 X = date code

**LINKS TO ADDITIONAL RESOURCES**

**FEATURES**

- Ultra compact DFN1006-2A
- AEC-Q101 qualified available
- Low package height
- 1-line ESD protection
- Working range -7 V up to +14 V or -14 V up to +7 V
- Low leakage current < 0.1  $\mu$ A
- Low load capacitance typical  $C_D = 8$  pF
- ESD immunity acc. IEC 61000-4-2
  - $\pm 25$  kV contact discharge
  - $\pm 30$  kV air discharge
- e3 - Sn
  - Tin plated exposed side wall of lead frame
  - Soldering can be checked by standard vision inspection
  - AOI = automated optical inspection
  - No X-ray necessary
- PATENT(S): [www.vishay.com/patents](http://www.vishay.com/patents)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**ORDERING INFORMATION**

| PART NUMBER<br>(EXAMPLE) | AEC-Q101<br>QUALIFIED | ENVIRONMENTAL AND QUALITY CODE                  |               | PACKAGING CODE                 | ORDERING CODE      |
|--------------------------|-----------------------|---|---------------|--------------------------------|--------------------|
|                          |                       | RoHS-COMPLIANT +<br>LEAD (Pb)-FREE TERMINATIONS | TIN<br>PLATED | 10K PER 7" REEL<br>(8 mm TAPE) |                    |
|                          |                       | GREEN   |               | MOQ = 10K                      |                    |
| VCUT0714BHD1             | -                     | G   | 3             | -08                            | VCUT0714BHD1-G3-08 |
| VCUT0714BHD1             | H                     | G   | 3             | -08                            | VCUT0714BHD1HG3-08 |

**PACKAGE DATA**

| DEVICE NAME  | PACKAGE NAME | PIN PLATING | TYPE CODE | WEIGHT  | MOLDING COMPOUND<br>FLAMMABILITY RATING | MOISTURE SENSITIVITY LEVEL           | SOLDERING CONDITIONS            |
|--------------|--------------|-------------|-----------|---------|---|--------------------------------------|---------------------------------|
| VCUT0714BHD1 | DFN1006-2A   | e3          | :A        | 0.83 mg | UL 94 V-0                               | MSL level 1<br>(according J-STD-020) | Peak temperature<br>max. 260 °C |

**ABSOLUTE MAXIMUM RATINGS**

| PARAMETER             | TEST CONDITIONS  | SYMBOL    | VALUE       | UNIT |
|-----------------------|--|-----------|-------------|------|
| Peak pulse current    | Pin 1 to pin 2, acc. IEC 61000-4-5, 8/20 $\mu$ s/single shot | $I_{PPM}$ | 3.6         | A    |
|                       | Pin 2 to pin 1, acc. IEC 61000-4-5, 8/20 $\mu$ s/single shot |           | 2           | A    |
| Peak pulse power      | Pin 1 to pin 2, acc. IEC 61000-4-5, 8/20 $\mu$ s/single shot | $P_{PP}$  | 50          | W    |
|                       | Pin 2 to pin 1, acc. IEC 61000-4-5, 8/20 $\mu$ s/single shot |           | 61          | W    |
| ESD immunity          | Contact discharge acc. IEC 61000-4-2; 10 pulses              | $V_{ESD}$ | $\pm 25$    | kV   |
|                       | Air discharge acc. IEC 61000-4-2; 10 pulses                  |           | $\pm 30$    | kV   |
| Operating temperature | Junction temperature; for AEC-Q101 qualified devices         | $T_J$     | -55 to +150 | °C   |
| Storage temperature   |  | $T_{stg}$ | -65 to +150 | °C   |

**PATENT(S):** [www.vishay.com/patents](http://www.vishay.com/patents)

This Vishay product is protected by one or more United States and international patents.

**CUT THE SPIKES**

The VCUT0714BHD1 is a bidirectional but asymmetrical (BiAs) ESD protection device which clamps positive and negative overvoltage transients to ground. Connected between the signal or data line and the ground the VCUT0714BHD1 offers a high isolation (low leakage current, small capacitance) within the specified working range of -7 V to +14 V or -14 V and +7 V. Due to the short leads and small package size of the tiny DFN1006-2A package the line inductance is very low, so that fast transients like an ESD strike can be clamped with minimal over- or undershoots.



22286

**ELECTRICAL CHARACTERISTICS (pin 2 to pin 1)**

 ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)

| PARAMETER                 | TEST CONDITIONS/REMARKS                    | SYMBOL        | MIN. | TYP. | MAX. | UNIT          |
|---------------------------|--|---------------|------|------|------|---------------|
| Protection paths          | Number of lines which can be protected     | $N_{channel}$ | -    | -    | 1    | lines         |
| Reverse stand-off voltage | Max. reverse working voltage               | $V_{RWM}$     | -    | -    | 14   | V             |
| Reverse voltage           | At $I_R = 0.1\text{ }\mu\text{A}$          | $V_R$         | 14   | -    | -    | V             |
| Reverse current           | At $V_{RWM} = 14\text{ V}$                 | $I_R$         | -    | -    | 0.1  | $\mu\text{A}$ |
| Reverse breakdown voltage | At $I_R = 1\text{ mA}$                     | $V_{BR}$      | 14.5 | -    | -    | V             |
| Reverse clamping voltage  | At $I_{PP} = 1\text{ A}$                   | $V_C$         | -    | -    | 27   | V             |
|                           | At $I_{PP} = I_{PPM} = 2\text{ A}$         | $V_C$         | -    | -    | 30   | V             |
| Capacitance               | At $V_R = 0\text{ V}$ ; $f = 1\text{ MHz}$ | $C_D$         | -    | 8    | 8.5  | pF            |
|                           | At $V_R = 7\text{ V}$ ; $f = 1\text{ MHz}$ | $C_D$         | -    | 4    | -    | pF            |

**ELECTRICAL CHARACTERISTICS (pin 1 to pin 2)**

 ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)

| PARAMETER                 | TEST CONDITIONS/REMARKS                    | SYMBOL        | MIN. | TYP. | MAX. | UNIT          |
|---------------------------|--|---------------|------|------|------|---------------|
| Protection paths          | Number of lines which can be protected     | $N_{channel}$ | -    | -    | 1    | lines         |
| Reverse stand-off voltage | Max. reverse working voltage               | $V_{RWM}$     | -    | -    | 7    | V             |
| Reverse voltage           | At $I_R = 0.1\text{ }\mu\text{A}$          | $V_R$         | 7    | -    | -    | V             |
| Reverse current           | At $V_{RWM} = 7\text{ V}$                  | $I_R$         | -    | -    | 0.1  | $\mu\text{A}$ |
| Reverse breakdown voltage | At $I_R = 1\text{ mA}$                     | $V_{BR}$      | 7.3  | -    | -    | V             |
| Reverse clamping voltage  | At $I_{PP} = 1\text{ A}$                   | $V_C$         | -    | -    | 13   | V             |
|                           | At $I_{PP} = I_{PPM} = 3.6\text{ A}$       | $V_C$         | -    | -    | 15   | V             |
| Capacitance               | At $V = 0\text{ V}$ ; $f = 1\text{ MHz}$   | $C_D$         | -    | 8    | 8.5  | pF            |
|                           | At $V = 3.5\text{ V}$ ; $f = 1\text{ MHz}$ | $C_D$         | -    | 6.4  | -    | pF            |

**TYPICAL CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)

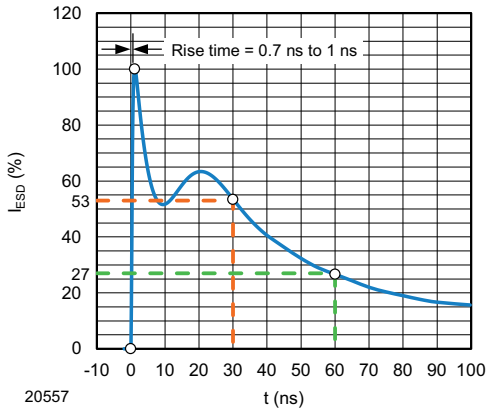


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330  $\Omega$ /150 pF)

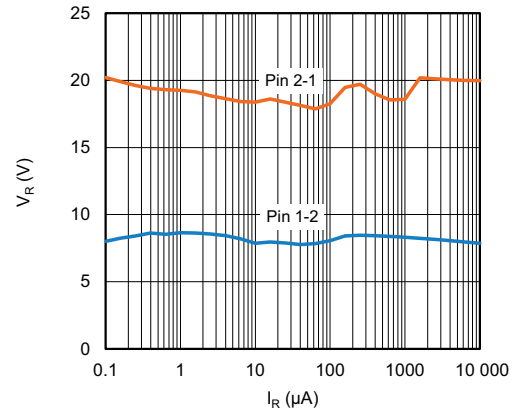


Fig. 4 - Typical Reverse Voltage vs. Reverse Current

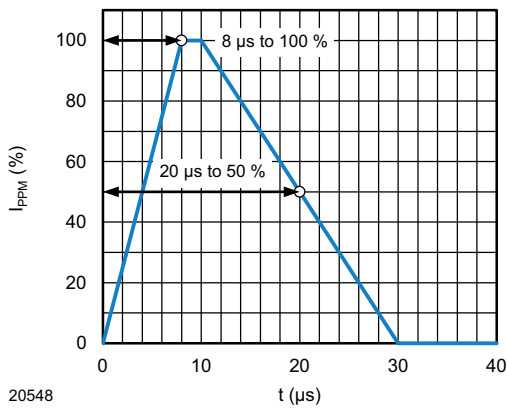


Fig. 2 - 8/20  $\mu\text{s}$  Peak Pulse Current Wave Form acc. IEC 61000-4-5

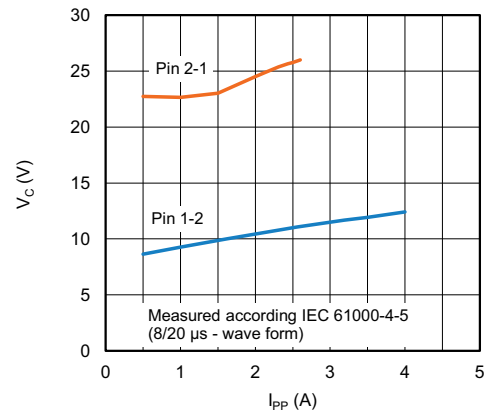


Fig. 5 - Typical Peak Clamping Voltage vs. Peak Pulse Current

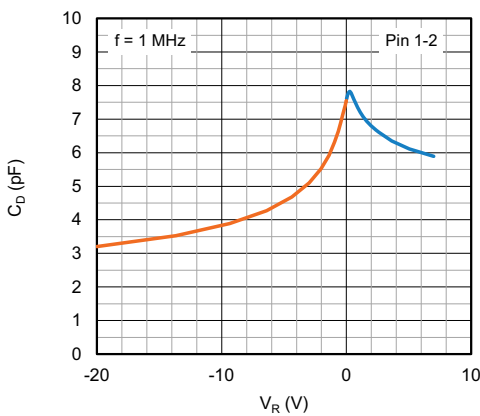


Fig. 3 - Typical Capacitance vs. Reverse Voltage

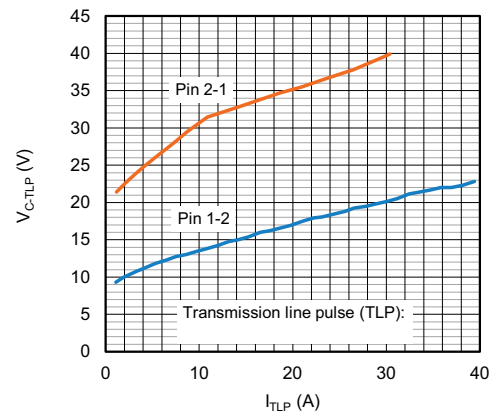
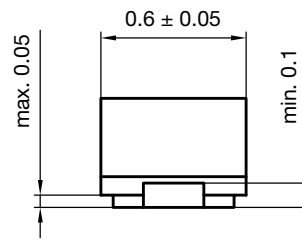
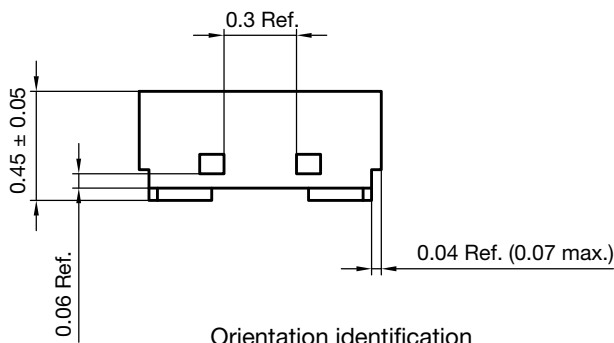
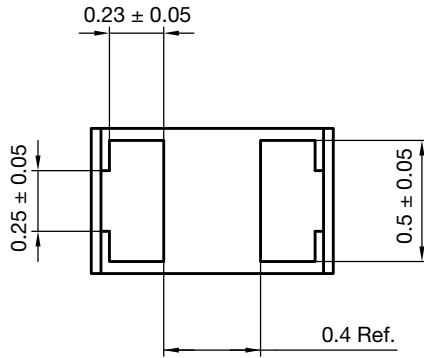


Fig. 6 - Typical Clamping Voltage vs. Peak Pulse Current

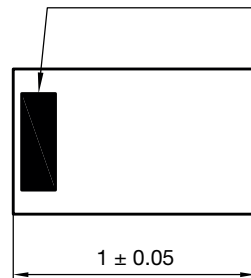


**PACKAGE DIMENSIONS** in millimeters (inches): **DFN1006-2A**

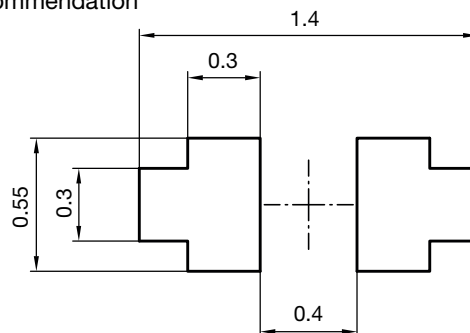
Package = Chip Dimension in mm



Orientation identification



Footprint recommendation

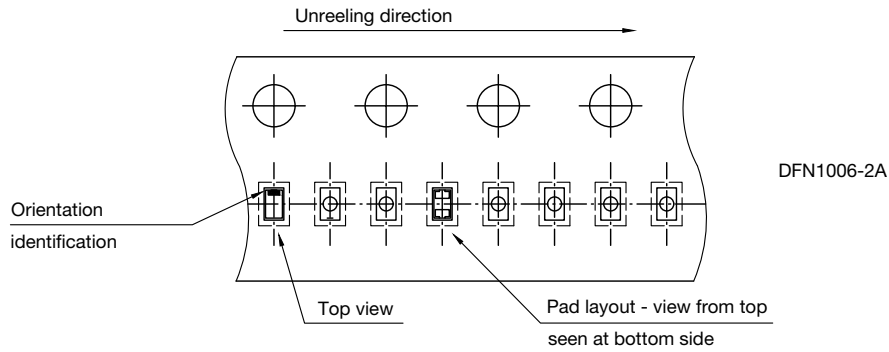


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**ORIENTATION IN CARRIER TAPE: DFN1006-2A**



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02.05.2017  
22965



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