SHARP SERVICE MANUAL

CODE : 00ZMZ5600SM/E

PERSONAL COMPUTER

MFM R-T P.6
8INCH circuit diagram

MODEL MZ-5600

CONTENTS

SHARP CORPORATION

1. MZ-5600 SERIES HARDWARE DESCRIPTION

1-1 System configuration

The following figure shows the complete system configuration for the MZ-5600 Series system, including some peripheral devices which are to be marketed in the near future.

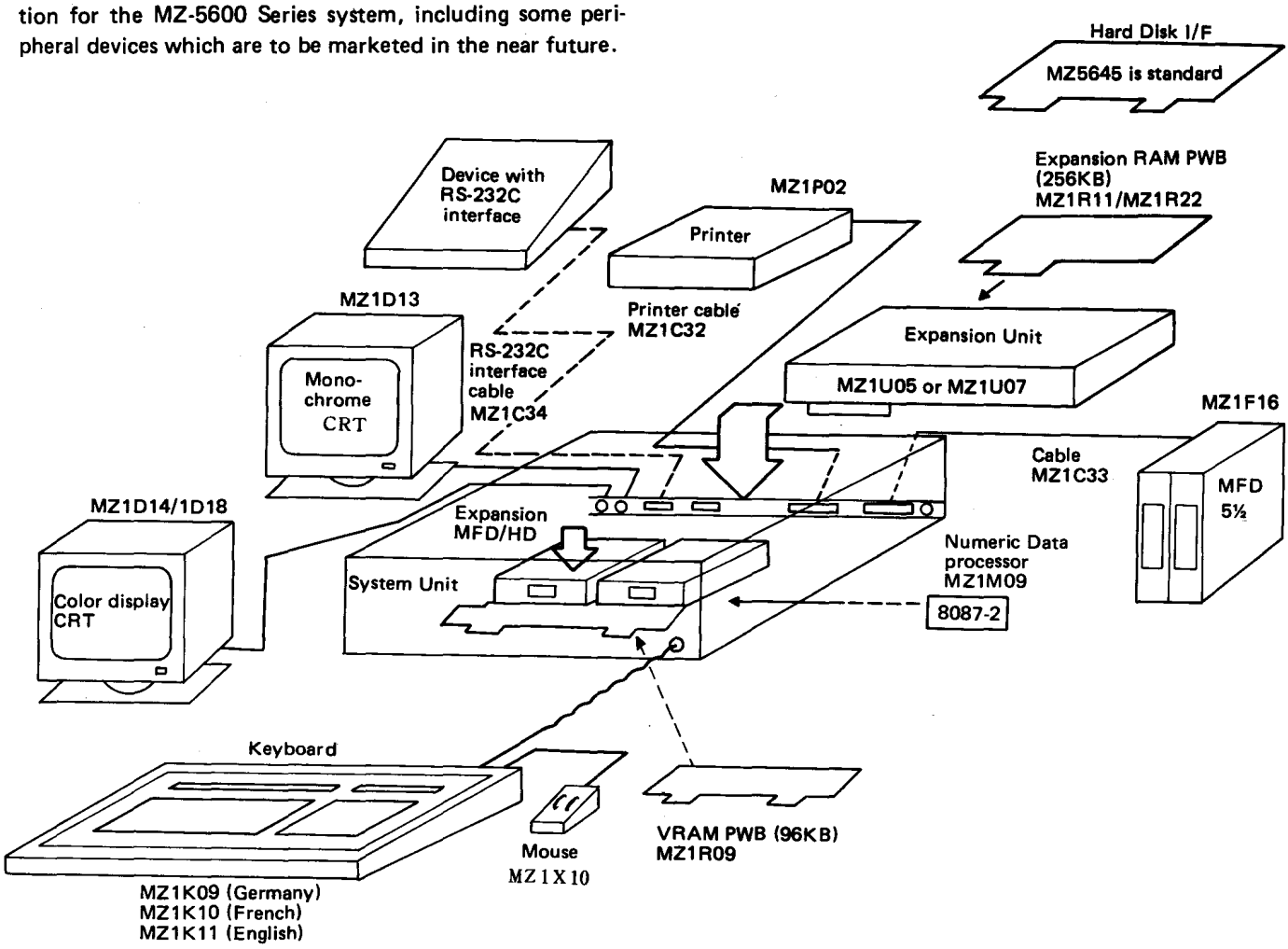


Fig. 1

1-2 Specifications

1-2-1 System highlights

1) High data processing capability achieved with a 16-bit microprocessor.
2) Large addressable memory space of 512KB: Standard 256KB plus an additional 256KB.
3) High-resolution color graphic display with large-capacity video screen memory and bit-map display.
4) One or two mini-floppy disk drives, each of 640KB are provided as a standard feature. And the MZ5645 is 10 MB Hard disk is standard.
5) Powerful standard I/O system interface.
6) Integrated sound generator.
7) CP/M86 as the standard operating system.

1-2-2 Model description

Model	Description
MZ-5631	Contains one MFD plus 256KB of RAM.
MZ-5641	Contains two MFD's plus 256KB of RAM.
MZ-5645	Contains one MFD and one HD plus 256KB RAM.

1-2-3 Specification of Disk

Item	HD	MFD
No, of side/drive	1	2
Tracks/side	673	40
Bytes/sector	512	256
Sectors/track	16	16
Total Bytes/Drive	5513216	327680
Bytes/block	4096	2048

1-2-4 Specifications

Table 2

Item		Std./Opt.			Description
CPU		Std. Opt. Std.	8086-2 (8 MHz) 8087-2 (8 MHz) 80C49	Main Numeric data processor. For keyboard control.	
MEMORY	ROM	Std.	IPL	16KB (8KB x 2)	
	RAM	Std. Std. Opt. Opt.	SYSTEM VRAM SYSTEM VRAM	256KB 96KB 256KB 96KB	Installed in the Expansion Unit. Available by a RAM PWB.
DISPLAY	I/F		Monochrome Color	Composite signal R.G.B.V.H SYNC	
	Display scheme			Bit map display	
	Screen configuration by system soft ware (CPM III)	Std.	Resolution Pages	B/W: 640 x 400, 2 pages 640 x 200, 6 pages 320 x 200, 12 pages C: 640 x 400, 1 page 640 x 200, 2 pages 320 x 200, 4 pages	
	Color			8 colors (can be specified for each dot)	
	Gradation			8 gradations available with the dedicated monitor.	Available on a monochrome monitor (1D13) with a 640 x 400 matrix.
	Screen/character configuration		Display capacity Character cell	40 or 80 characters on each row. The number of rows per screen is programmable. 8 x 8, 8 x 16	Controlled by software.
	Screen control		Superimposed Multi-window Scroll Reduction/ expansion Palette feature Background color Color priority Reverse video Boundary color	3 pages 4 windows Character scroll Smooth scroll Software control 8 colors available Can be specified for each window. Planes with order of priority. Reversible for each window.	Horizontal or vertical direction. Vertical direction only. 8 colors Available on all color models other than the 640 x 400 dot model.

Table 2

Item		Std./Opt.			Description
Integrated I/O interface	Sound	Std.		Three codes available through a built-in speaker.	
	Centronics I/F	Std.		One channel	For printer attachment.
	Clock	Std.	Real-time clock	Backed up by battery.	Built-in 13 byte RAM.
	MFD I/F	Std.		Capable of controlling up to 4 drives.	Two built-in drives plus two external drives.
	RS-232C	Std.	A Channel	Start-stop asynchronous/sync.	Programmable between 110 and 9600 bauds.
		Std.	B Channel	Start-stop asynchronous.	
	Key I/F	Std.			
OP I/O I/F	256KB RAM PWB	Opt.		Expansion RAM PWB.	For MZ5631
	HD I/F PWB	Opt.		Hard disk drive I/F PWB.	MZ5645 is standard
	Expansion Unit	Opt.			
Additional device	Mouse	Opt.		Attached to keyboard.	
	MFD	Opt.	Single drive increment.	Additional drive to be installed in the System Unit.	For MZ5631 only
	MFD unit	Opt.	Contains two drives.	External drives	Available with the MZ-1F16
	Hard disk unit	Opt.		10M Bytes	MZ1F10 External M Internal
CRT	12" monochrome	Opt.		640 x 400 dot matrix	MZ-1D13
	12" color display	Opt.		640 x 400 dot matrix	MZ-1D14
	15" color display	Opt.		640 x 400 dot matrix	MX-1D18
Printer	80 columns	Opt.			MZ-1P02

1-2-5 Optional devices specifications

* Green monitor MZ-1D13

Table 3

Type	High resolution 12" monochrome video monitor for the MZ-5600 Series	
Specifications	CRT	12 inches, 90 deg. deflection
	Display capacity	640 dots horizontally by 400 rasters vertically
	Input signal	Composite signal of 1 Vp-p
	Supply voltage	Rated voltage
	Power consumption	*29 Watts
	Outer dimensions	313(W) x 289(H) x 327(D)mm
	Weight	6.2kg

* Color monitor MZ-1D14

Table 4

Type	High resolution color video monitor for the MZ-5600 Series	
Specifications	CRT	12 inches, 90 deg. deflection
	Display capacity	640 dots horizontally by 400 rasters vertically
	Video input signal	Independent RGB input of TTL level with positive polarity
	Sync. input	Independent H.V. sync. inputs of TTL level with negative polarity
	Supply voltage	Rated voltage
	Power consumption	*63 Watts
	Outer dimensions	326(W) x 288(H) x 375(D)mm
	Weight	11kg

* Expansion Unit MZ-1U07/1U05

Table 5

Description	Used to install optional expansion PWBs or interface PWBs required to control optional peripheral devices which cannot be controlled with the interface contained in the MZ-5600 Series System Unit. (MZ1U05 is 4 slots and MZ1U07 is 5 slots.)

* Expansion RAM PWB MZ-1R22/1R11

Table 6

Description	Designed to be installed in the expansion Unit to add 256KB of additional RAM space. (MZ1R22 is used only SEEG)

* Expansion VRAM PWB MZ-1R09

Table 7

Description	Provides an additional VRAM space of 96KB to increase the total VRAM area to 192KB for extended graphic capabilities.

* Arithmetic and logical processor MZ-1M09

Table 8

Description	Designed to increase arithmetic and logical operation speeds. (8087-2)

* Additional mini-floppy disk drive (MFD) MZ-1F16

Table 9

Description	Additional mini-floppy disk drive unit for the MZ-5600 Series. May be used as the 3rd and 4th drives, and has a total storage capacity of 1280 KB. Join to the MFD I/F connector on the rear of the System Unit using the dedicated cable MZ-1C43. (FD55F)		
Specifications	Drive	Thin-profile, double-sided, double-density drive (FD55F) x 2.	
	PWB	I/F PWB: 45 x 129mm (double-sided paper epoxy board)	
		LED PWB: 23 x 8.5mm (single-sided paper epoxy board)	
	Power supply	Switching regulator	+5V (1.3A) and +12V (1.3A) Contained in a metallic housing measuring 98(W) x 16.5(H) x 87(D)mm
	Cabinet	Top and bottom cabinets: Press-molded metal Front panel: Molded resin Color: Office gray Dimensions: 117.7(W) x 177.7(H) x 331.3(D)mm Weight: 6kg	

Color Display MZ1D18

Table II

Product outline	640 x 400 dots, 15 inch flat square, non-glare semi-black type color display for use with the MZ-5600.		
Specification	Tube used	15 inch, 90° deflection flat square type (non-glare treated)	
	Input signal (Horizontal synchronization signal) (Vertical synchronization signal)	R, G, B, three independent TTL polarity TTL positive polarity TTL negative polarity	
	(Deflection frequency)	24.86KHz, horizontal, and 55.48 Hz, vertical	
	Display time	29.80μS, horizontal and 16.09 ms, vertical	
	Resolution	640 dots, horizontal, and 400 dots, vertical	
	Display colors	Seven colors of red, green, blue, yellow, magenta, cyan, white, and black	
	Display capacity	4000 characters, maximum. 2000 characters with the MZ-5600.	
	Dot pitch	0.39 mm	
	Power supply	Rated voltage	
	Physical dimensions	404(W) x 409(D) x 331(H) mm	
	Weight	15.0 Kg	
	Power consumption	75 (W)	
	Input connector	Rectangular 8-pin connector 1. Open 2. Video input (red) 3. Video input (green) 4. Video input (blue) 5. Ground 6. Ground 7. Horizontal synchronizing signal 8. Vertical synchronizing signal	
	Adjust knob	Front	POWER switch
		Side	Vertical synchronization, vertical amplitude, horizontal synchronization, horizontal phase, brightness
	System configuration	[Personal computer] MZ-5600 series ↓ [Color display] MZ-1D18 (Cable attached to the unit) ↓ [Tilt stand]	
	Appearance color	Office gray	
Accessories	Interfacing cable, instruction manual		

* Printer

Table 10

Model	Print system	Max. print speed	Character type	Character cell	Max. columns/row	Max. paper width/feed method	Copy capacity
MZ-1P02	Dot matrix impact printer	120cps	Alphanumeric, and symbolic, characters	Basic: 9 columns x 9 rows Character: 9 columns x 7 rows	Standard 80 characters	10 inches/ • Friction feed • Tractor feed (optional)	3 copies, conditional

1-3 System configuration

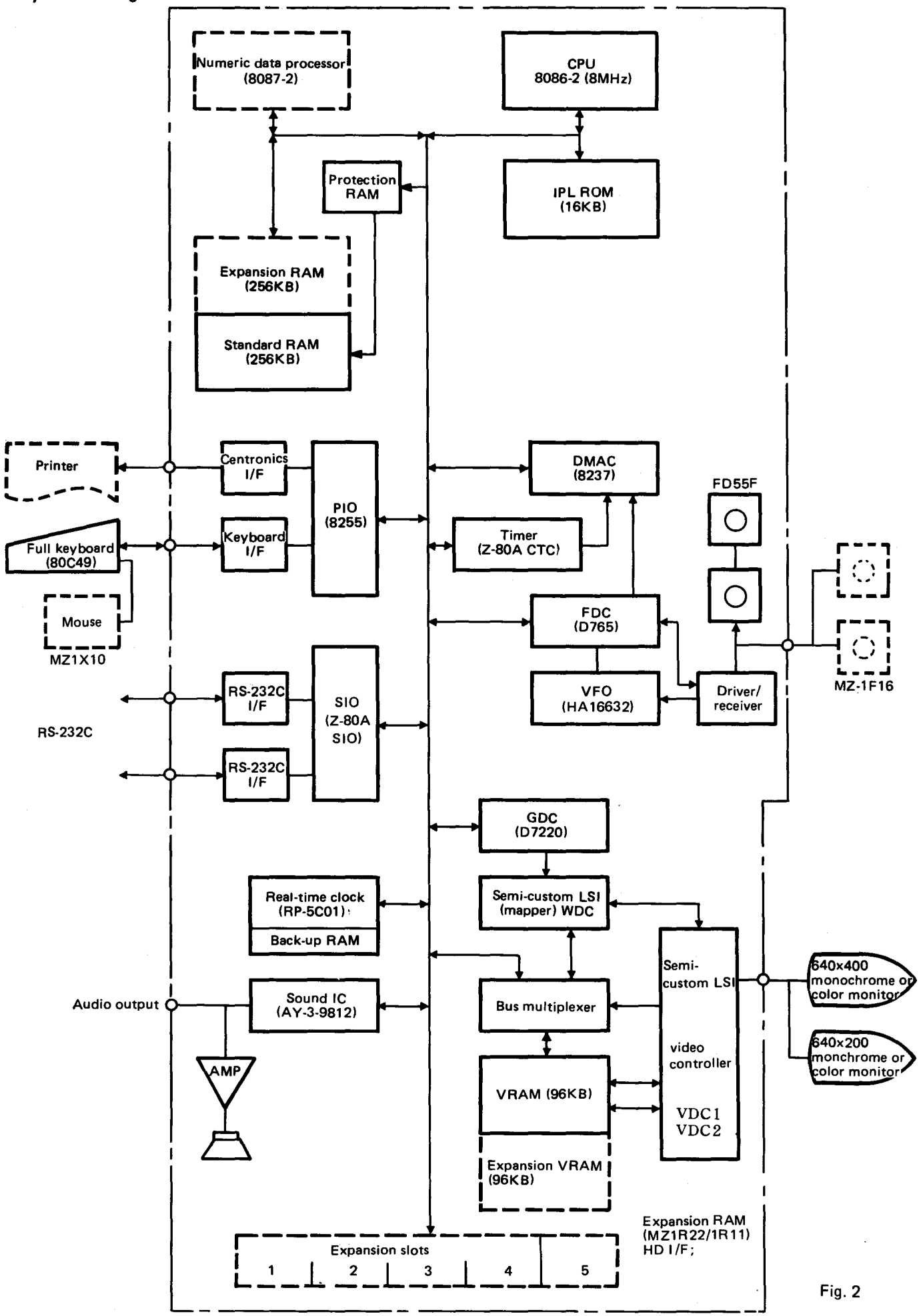
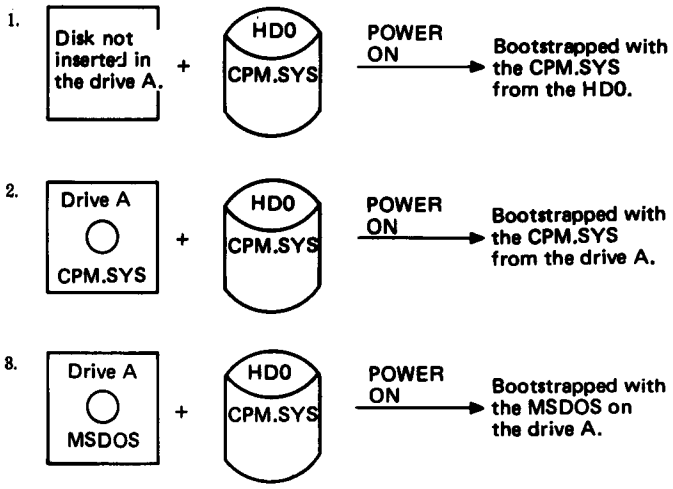


Fig. 2

2. SOFTWARE CONFIGURATION

2-1 System bootstrap

It becomes possible with the MZ-5600 to bootstrap from the hard disk when the CPM.SYS or MSDOS is stored on the hard disk, provided that the following restriction is applicable.
"The system file (CPM.SYS or MSDOS) can only be loaded from the physical drive unit number 0 during IPL."
If the CPM.SYS has been stored in the HD0, for instance;



Thus, it becomes necessary to store the MSDOS after erasing the CPM.SYS on the HD0, inorder to bootstrap the MSDOS from the hard disk.

SYSTEM DISK

DEVICE	SYSTEM DISK	
640KB MFD	O	Must be created by DSKMAINT.
HD	O	Must be created by DSKMAINT.
320KB MFD	X	Creation and bootstrap are not possible.
SFD	X	Creation and bootstrap are not possible.

640KB MFD format

256 bytes/sector
16 sectors/track
80 tracks/side

2K bytes/block
128 directory entries

* Prior to the use of a fresh disk, it becomes necessary to format the disk using DSKMAINT.

2-2 CP/M-86

Logical drive map

	Logical drive	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1		640KB MFD				SFD				HD		N.U		MD	SFD	320KB MFD
	Physical drive	0	1	2	3	0	1	2	3	0		1		0	0	0 ~ 3
2		HD		↑		↑				↑		↑		↑		
	Physical drive	0														

1) Setup for above 1 or 2 is possible using IOCNF utility program.
2) M represents the memory disk.
3) N supports the SFD0 of the one-sided, single density.
4) O supports MFD0-3 as 320/640 KB MFD. For kind of the disk supported, refer to instruction book, DSKCNV. But drive O can only be read. If write is tried to a 320 KB disk, it evokes a BDOS error.

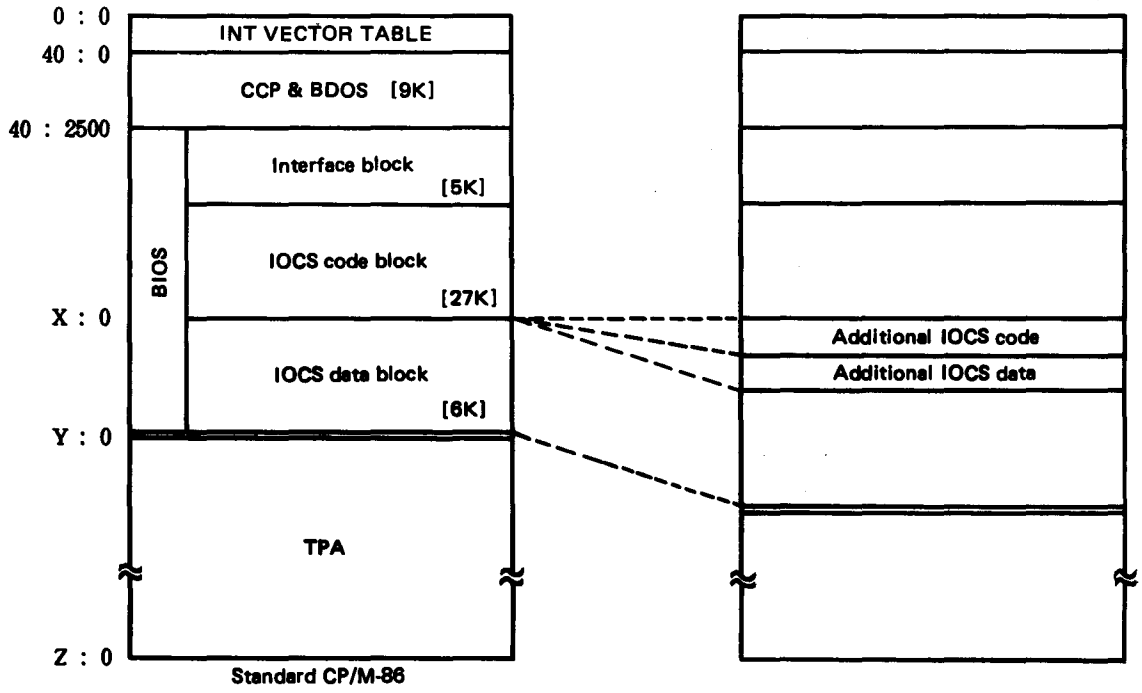


Fig. 3

Fig. 4

The above figure provides the memory map for the CP/M-86 used on the MZ-5600.
The BIOS consists of the following three blocks:

i) Interface block: Interfaces the BDOS with IOCS.
ii) IOCS code block: Control program for the input output device handler called the Input Output Control System (IOCS).
iii) IOCS data block: Parameter and work area used for the IOCS.

The MZ-5600 system can be upgraded by using an INSTALL command which integrates the optional IOCS module into the BIOS. The above figure on the right provides the memory map for the upgraded system:

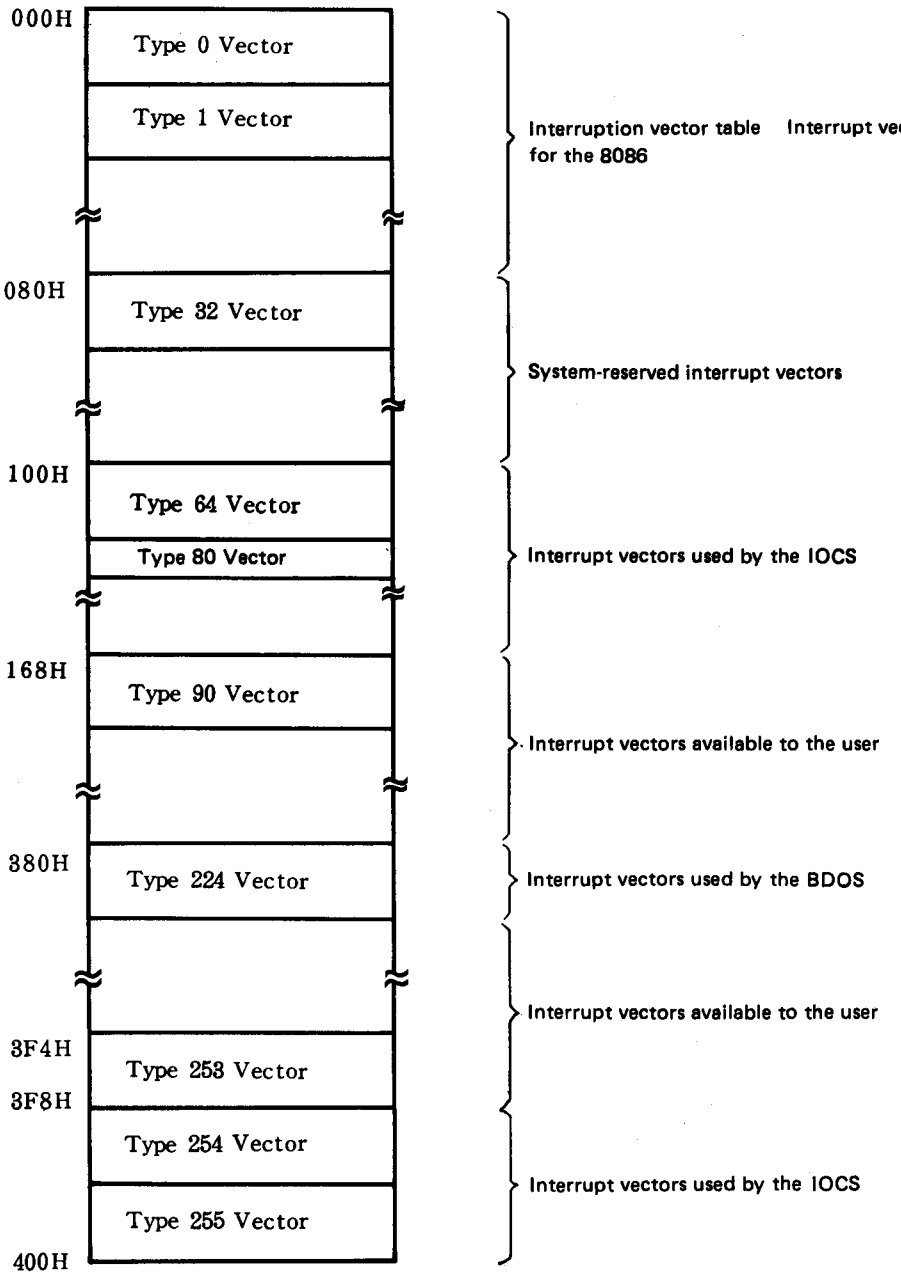


Fig. 5

CP/M-86 transient command set

ASM86:	Assembler for the 8086
GENCMD:	Command file production utility
DDT86:	Dynamic debugging tool
ED:	Editor
PIP:	File merge and transfer utility
STAT:	File and disk status display utility
SUBMIT:	Batch processing utility
HELP:	Command usage display utility
DSKMAINT	FORMAT
	COPYDISK
	COPYFILE
	COPYSYS
	VERIFY
TOD:	Time and date set-up and display utility
KEY.	Definable key set-up utility
RSPARM.	RS-232C parameter set-up utility
ASSIGN:	Logical/physical device allocation utility
IOCNF:	I/O configurator
INSTALL:	System install utility
KEYNO:	Reads Key Board Controller version number.
ROMNO:	Reads ROM IPL version number.
PATCH:	Patch and dump
FCOPY:	Copy from 2D type disk.

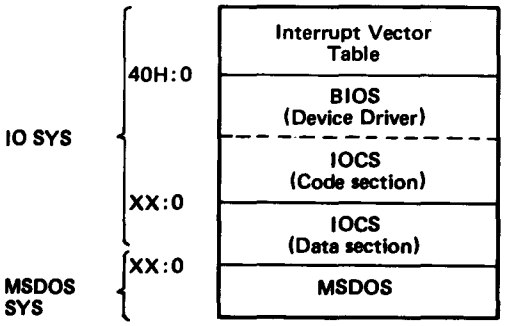
Hard disk utilities

Hard disk utilities	BFMT:	Backup floppy format
	BKUP:	Backup
	BRST:	Backup restore
	BERA:	Backup floppy erase
	HDTRNS:	Hard retract for transporty

2-3 MS-DOS

1) Memory map

The MS-DOS memory is mapped as illustrated below. BIOS, IOCS and SYSINIT are linked on the HP in their given order and comprise IO SYS.



2) MS-DOS commands

(a) Disk control commands

Command name	In/Out	Function
CHKDSK	Out	Analysis the directory and FAT and checks the state of the disk.
DISKCOPY	Out	Duplication of a whole disk contents
FORMAT	Out	Disk initialization, volume label write, system file copy, etc.
VOL	In	Display of volume label

(b) Directory and file control commands

Command name	In/Out	Function
CHDIR	In	Changing or displaying the current directory contents
COPY	In	Duplication of the specified file
DEL	In	Deletion of the specified file
DIR	In	Displaying of the directory
MKDIR	In	Creation of directory
PATH	In	Providing the pass to trace the command
RECOVER	Out	Recovery of the file or directory
REN	In	Changing the file name
RMDIR	In	Deleting the directory
FC	Out	Comparison of two files
TYPE	in	Displaying of the contents of the specified file

(c) System operating commands

Command name	In/Out	Function
BREAK	In	Changing the break interrupt check range
CLS	In	Clear of the screen
CTTY	In	Change of i/o device
DATE	In	Display or set of the date
EXIT	in	Return to the program which initiated the command
FIND	Out	Search of the character string
MORE	Out	Output of screen one at a time
PRINT	Out	Printer output from the background
PROMPT	In	Setting command prompt
SET	In	Changing the value of the character string
SORT	Out	Rearranging the data in the alphabetical order or reverse alphabetical order
TIME	In	Display or setup of the time
VER	In	Displaying of the MS-DOS version number
VERIFY	In	Verifying the disk contents

(d) Program developing commands

Command name	In/Out	Funcition
EXE2BIN	Out	Changing the EXE file to the COM file
EDLIN	Out	Line editor
MASM	Out	Macro assembler
LINK	Out	Linker
LIB	Out	Library manager
CREF	Out	Creation of cross reference

(e) Batch processing commands

Command name	In/Out	Function
ECHO	In	Choice is made if the command were to be displayed during execution of the batCh program
FOR	In	Command is repeated to execute while substituting with the specified element
GOTO	In	Moves to the line in which the control specified label is existing
IF	In	Executes the command when the specified condition is true
PAUSE	In	Temporary halt of the batch process
REM	In	Displaying of the comment
SHIFT	In	Shifts the parameter allocations (expanded use of parameters)

(f) Other commands unique to the MZ-5600.

Command name	In/Out	Function
KEY	Out	Sets or changes the definable key function
INSTALL	Out	System installation is done to the printer and option devices
IOCNF	Out	Saves BIOS parameter, assigns or deassigns the read-after-write check to the floppy disk, computers memory disk logical drive number and physical drive number
MODE	Out	Input/output unit mode setup
ASSIGN	Out	Performs drive unit assignment
BKUP	Out	The contents of the hard disk is backed up on the floppy disk
BRST	Out	The hard disk data are restored from the backup floppy disk

3) Logical drive map

Logical drive	A	B	C	D	E	F	G	H	I	J	M	Q	R
Device	MFD		HD		SFD				MFD			MFD	
Physical drive	0	1	0		0	1	2	3	2	3	–	0	

↑
Memory disk

2-4 Memory map

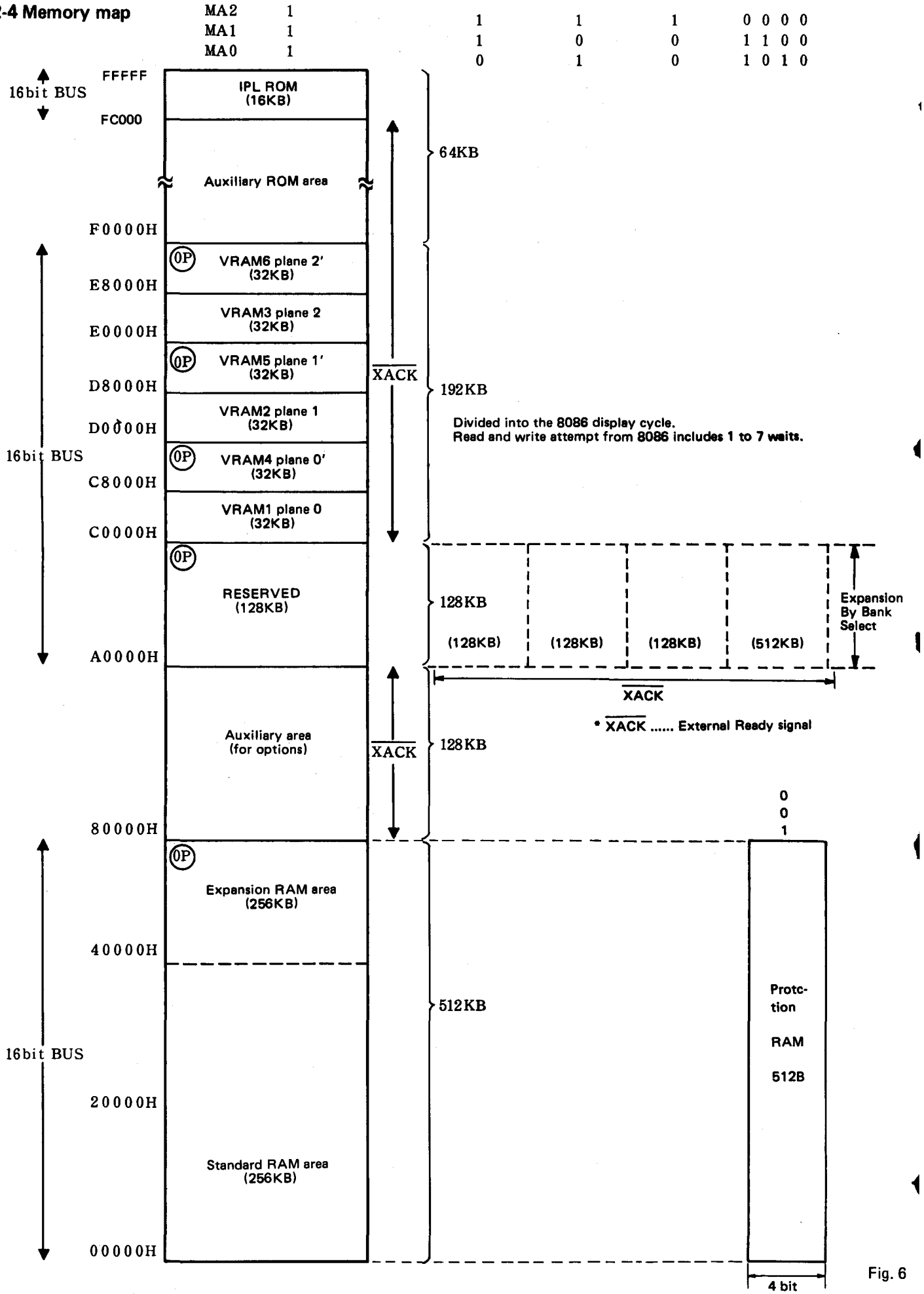


Fig. 6

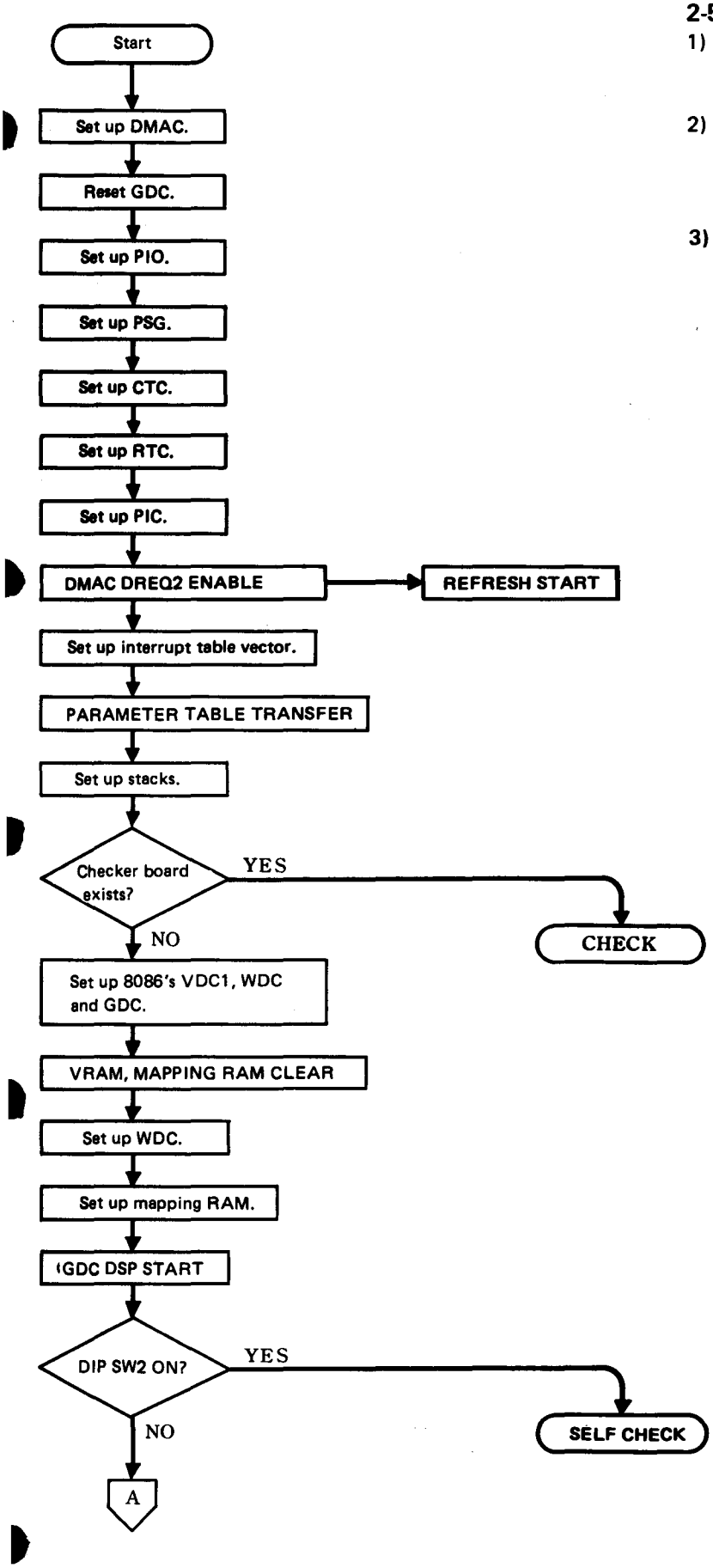


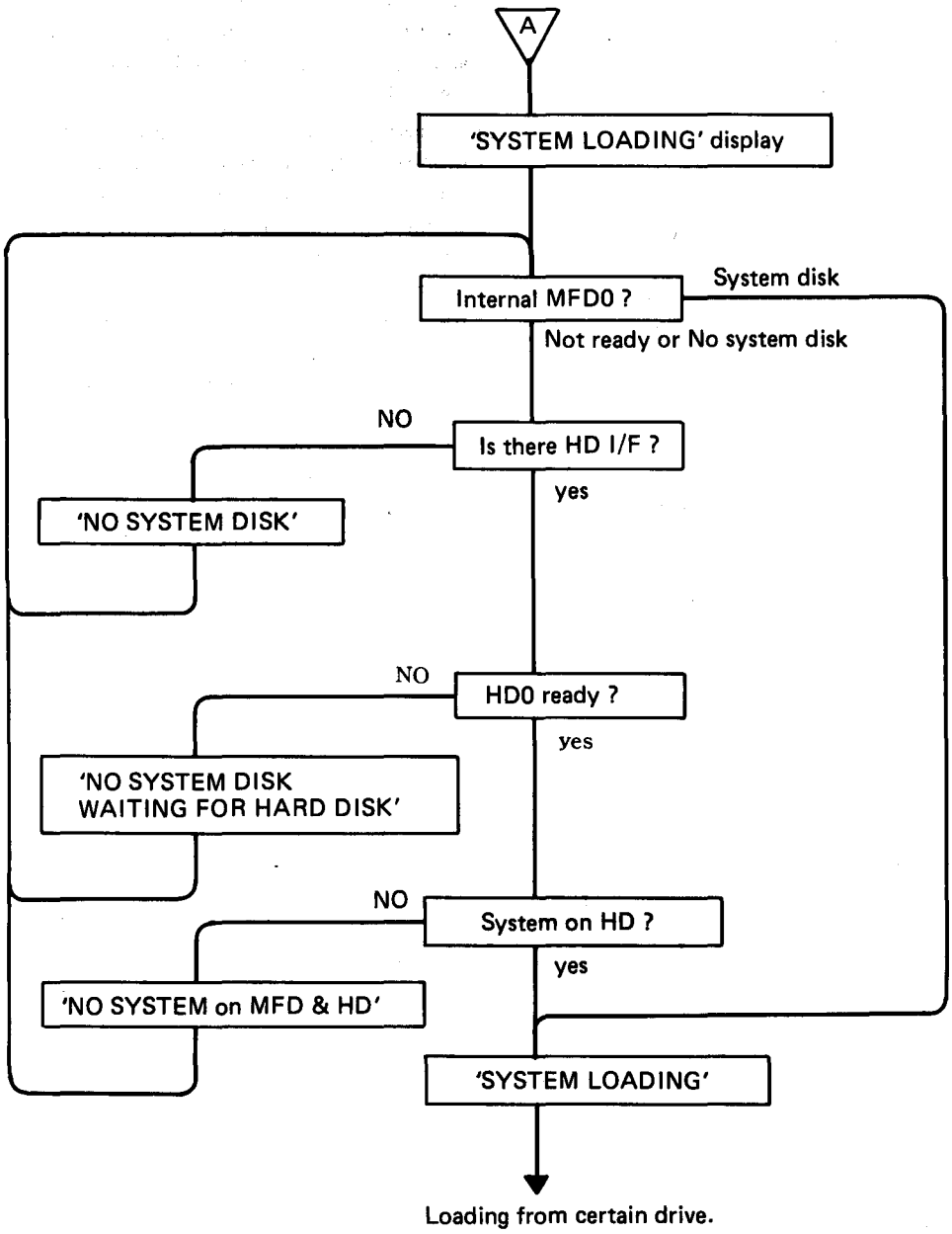
Fig. 7

2-5 IPL sequence

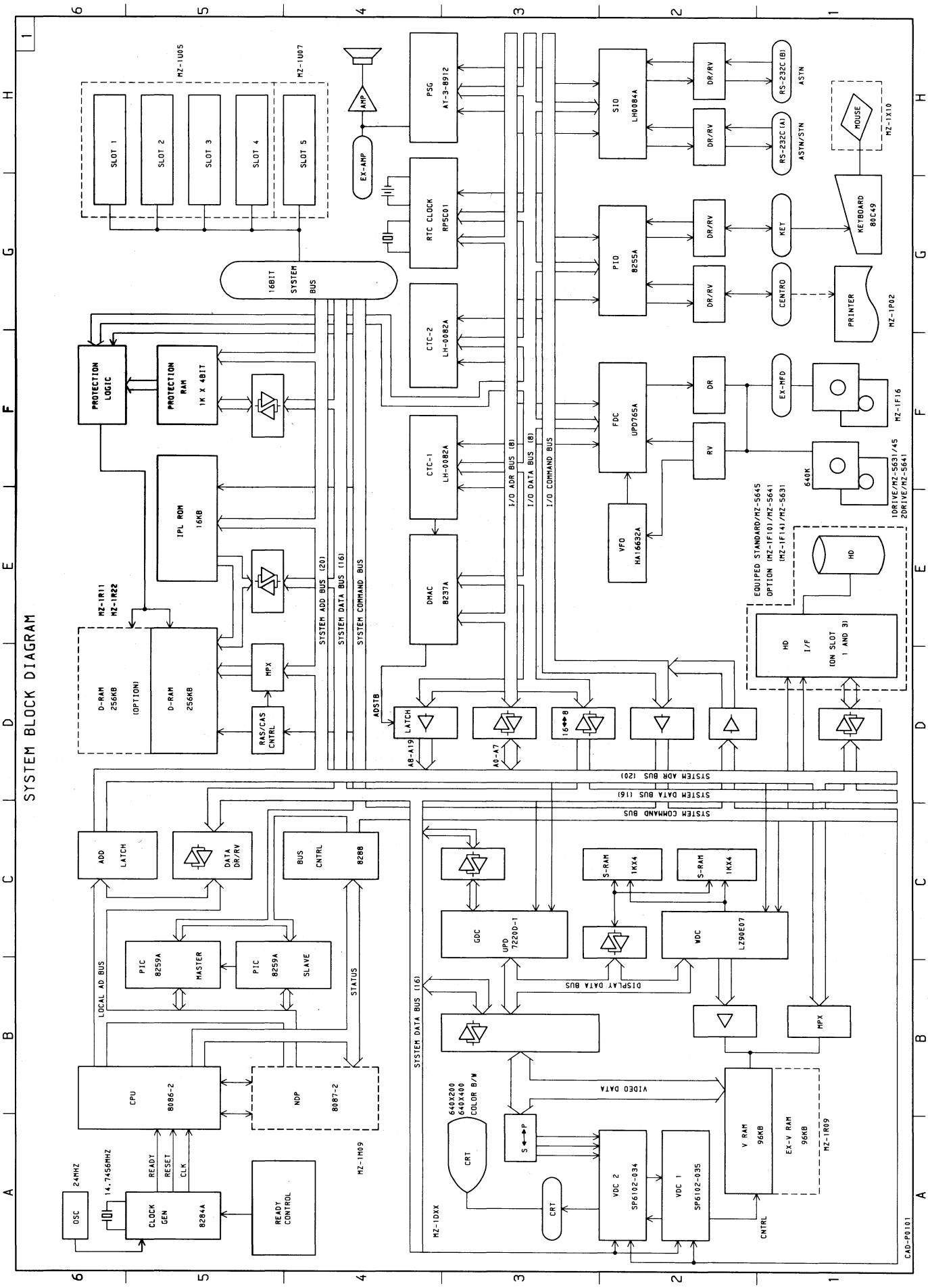
1) When the MZ-5600 system is powered up, the IPL program contained in the ROM is automatically initiated to execute the following sequence.
2) If section 2 of the DIP switch is ON, the system enters the Check mode (see the description of Check mode). In any other case, the system proceeds with the following step (3).
3) A message "SYSTEM LOADING" appears on the video monitor, and the loader is loaded from Drive zero into the system according to the information contained on sector 1 of track 0. When loading is completed, control skips to the first address of the loader.
   If an error occurred during loading, the system provides the following message display and waits until a new diskette is placed in the drive. When the new diskette is inserted, the system resumes the loading sequence.
   i) If no disk is placed in the drive or the diskette in the drive is not the system diskette:
      NO SYSTEM DISK
   ii) If a failure occurred in the disk or drive:
      ERROR WHILE LOADING

SYSTEM BOOT

It is possible to boot from the internal MFD "0" or HD "0".



3. MZ-5600 SYSTEM BLOCK DIAGRAM



4. THE CPU AND LSI PERIPHERAL LOGICS

4-1 General

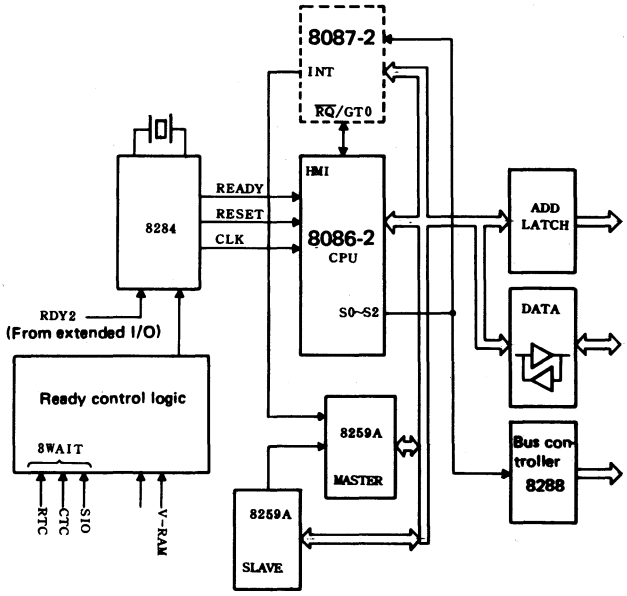


Fig. 10

The peripheral chips directly connected to the CPU (8086) include: — the 8284 for clock, reset and ready control; the 8259 for interrupt control; the 8288 for bus control, address latches, and data bus buffers.
The following describes these peripheral logics along with the CPU (8086) itself.

4-2 8086-2 microprocessor (16-bit parallel)

Highlights

(1) 16-bit parallel processing capability.
(2) Basic instruction set consisting of 90 instructions.
(3) Directly addressable 1MB memory space.
(4) 14 x 16 bit register set.
(5) 8 or 16-bit arithmetic operation (including multiplication and division) with or without sign.
(6) 8MHz single-phase clock.
(7) Maskable (INTR) or non-maskable (NMI) external interrupt input.
(8) Dual mode operation (minimum/maximum). (MZ5600 is used maximum)
(9) N-channel MOS.
(10) Single +5V power supply.
(11) 40 pins DIP package.

Pin configuration (top view)

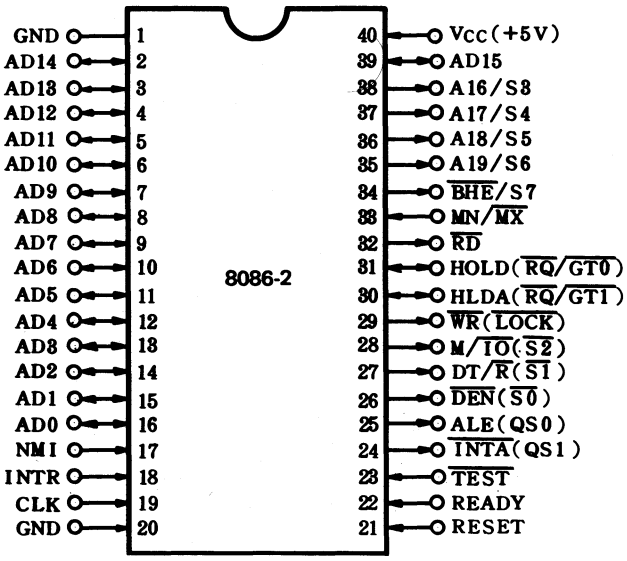


Fig. 11

Terminal names given in parentheses are used for the maximum mode. The MZ-5600 uses the 8086 in the maximum mode.

8086 functional outline

The 8086 has maximum and minimum modes, so that different pin configurations may be selected depending on the scale of the system used. The 8086 is internally divided into an execution unit (EU) and bus interface unit (BIU). The BIU controls a six-byte instruction queue and generates address information, while the EU interprets and executes instructions. Each unit operates asynchronously, and a large amount of processing is achieved with the pipeline processing scheme. The 8086 can directly access up to 1MB of memory space. Also it can handle data byte-by-byte (8 bits) or word-by-word (16 bits) depending on the status at the A0 and BHE terminals, to achieve efficient use of memory.

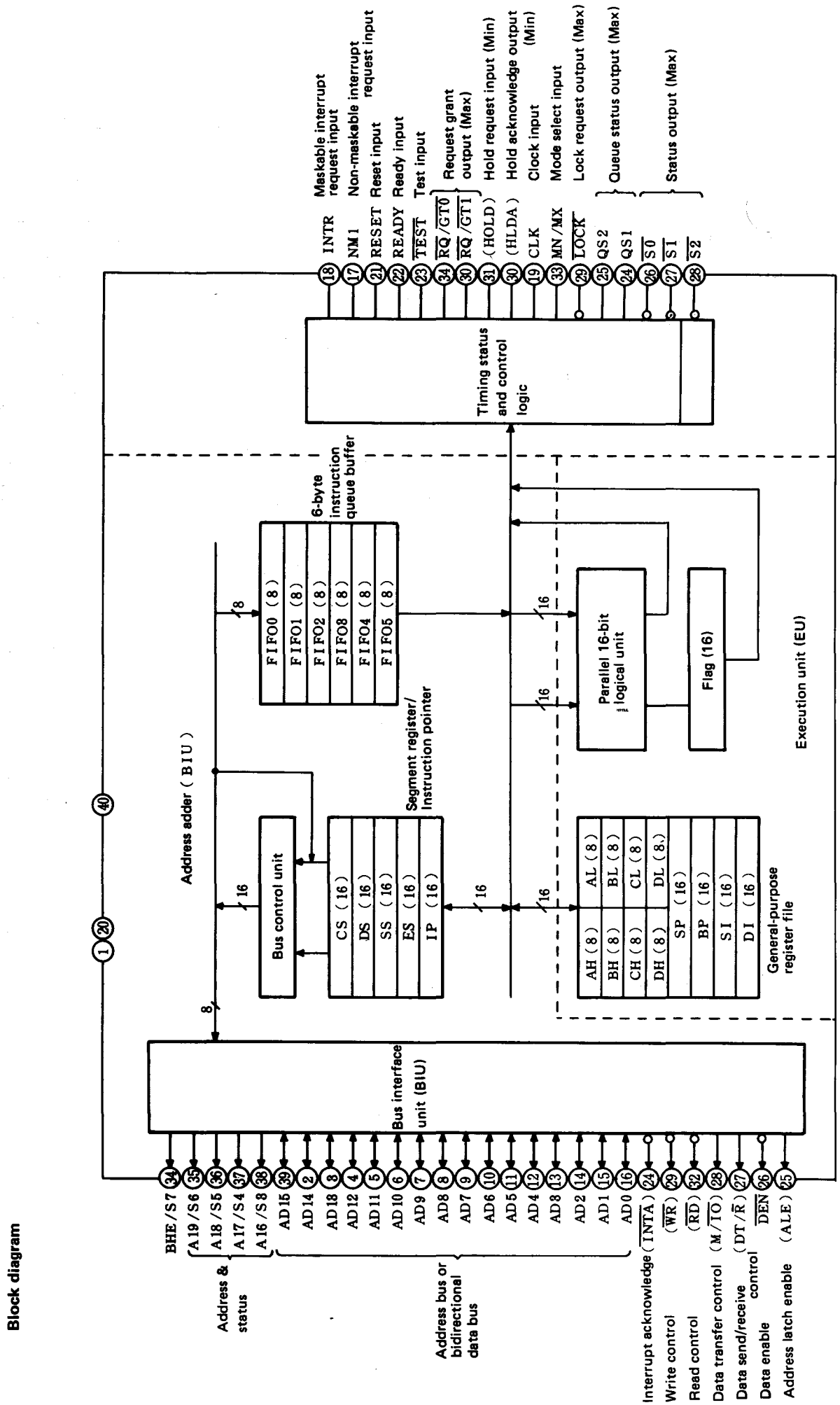


Fig. 12

Pin functions

Pins having the same function in both Max. and Min. modes.

Table 11-a

Pin No.	Pin name	Function	IN/OUT	Description
2~16 39	AD0~AD15	Address/data bus	IN/OUT	Used as address (A0—A15) and data (D0—D15) buses by time-division multiplexing.
35 ≀ 38	A19/S6 ≀ A16/S3	Address/status outputs	OUT	Outputs the most significant 4 bits (A16—A19) of address information or status information (S3—S6) by the time-division multiplexer. Address is output during T1 state, and status is output during T2, T3, TW, and T4 states. Bits S3 and S4 indicates which segment register is used for the current bus cycle. S4 S3 0 0 Extra segment 0 1 Stack segment 1 0 Code segment or no segment used 1 1 Data segment Bit S5 is an interrupt enable flag, and is updated at the beginning of each clock cycle. Bit S6 is always zero.
34	$\overline{BHE}$/S7	Bus high enable/ status output	OUT	Outputs bus high enable or status information by time-division multiplexing. Bus high enable is output during T1 state, while status information is output during T2, T3, TW, and T4 states. The bus high enable, in conjunction with A0, enables selection between byte-by-byte and word-by-word data handling. $\overline{BHE}$ A0 0 0 Word-by-word (16 bits) 0 1 High order byte 1 0 Low order byte 1 1 Not used.
32	$\overline{RD}$	Read control output	OUT	Active low output to indicate the timing of read operation from memory or I/O ports.
22	READY	Ready input	IN	Indicates that the memory or peripheral device is ready for data communication. If this is low, the CPU completes the current read or write cycle after it is set high.
18	INTR	Maskable interrupt request input	IN	Level sense terminal sampled at the last clock cycle of each instruction. This input is maskable with the program, and is used, in conjunction with the 8259A, to request 256 type vector interrupts.
23	$\overline{TEST}$	Test input	IN	The CPU samples this input by executing the WAIT instruction. If the Test input is low, the CPU continues the current execution; if it is high, the CPU repeats the idle cycle until the input is set low.
21	RESET	Reset input	IN	Used to initialize the internal logics of the CPU. This input must be maintained at high for at least 4 clock cycles.
17	NMI	Non-maskable interrupt request input	IN	Non-maskable, edge trigger interrupt input sampled by the last clock of an instruction execution cycle. Used for emergency interrupt such as power down, and causes a type 2 interrupt.
19	CLK	Clock input	IN	Accepts an external clock source, usually the 8284A clock generator.
33	$\overline{MX}$/MN	MAX/MINI	IN	Maximum/minimum mode select input

Pin used for minimum mode.

Table 11-b

Pin No.	Pin name	Function	IN/OUT	Description
28	M/$\overline{IO}$	Data transfer control output	OUT	Indicates whether the CPU is accessing the memory or an I/O device.
29	WR	Wirte control output	OUT	Indicates the timing of write operations to an external memory or I/O device.
24	$\overline{INTA}$	Interrupt acknowledge output	OUT	Used as a strobe to read interrupt vectors on the data bus during the interrupt acknowledge cycle. Also indicates an interrupt acknowledge to the device in request for interrupt.
25	ALE	Address latch enable output	OUT	Strobe used to load address information (which is output from the CPU on time-division scheme) into external latches.
27	DT/$\overline{R}$	Data send/receive control output	OUT	Indicates the direction of data transfer to an external data bus buffer.
26	$\overline{DEN}$	Data enable output	OUT	Enables the external data bus buffer.
31	HOLD	Hold request input	IN	When receiving a Hold request, the CPU relinquishes bus access authority and enters the Hold state immediately after completing the current machine cycle.
30	HLDA	Hold acknowledge output	OUT	Indicates that the CPU acknowledged the Hold request and relinguished bus access authority, to the device in request.

Pins used for maximum mode.

Table 11-c

Pin No.	Pin name	Function	IN/OUT	Description
26 ≀ 28	$\overline{S0}$ $\overline{S2}$ $\overline{S1}$	Status output	OUT	S2 S1 S0 0 0 0 Interrupt acknowledged. 0 0 1 Read I/O port. 0 1 0 Write I/O port. 0 1 1 Hold 1 0 0 Fetch instruction. 1 0 1 Read memory. 1 1 0 Write memory. 1 1 1 Passive cycle.
30, 31	$\overline{RQ}$/$\overline{GT0}$ $\overline{RQ}$/$\overline{GT1}$	Request/grant input/output	IN/OUT	Used to receive Hold request and output Hold acknowledge when a device other than the CPU wants to use the local bus. The $\overline{RQ}$/$\overline{GT0}$ pin has a higher priority over the $\overline{RQ}$/$\overline{GT1}$ pin.
29	LOCK	Lock request output	OUT	Used to inhibit other system bus masters accessing the system bus when the CPU wants to use the system bus.
24, 25	QS1, QS0	Queue status output	OUT	Indicates operations performed at the instruction queue: QS1 QS0 0 0 No operation. 0 1 Fetches the first byte (OP code) of an instruction. 1 0 Clears the contents of the queue. 1 1 Fetches the second and subsequent bytes of the instruction.

4-3 8284 clock generator and driver

Highlights

(1) Quartz-controlled oscillator with stable output frequency.
(2) External clock input.
(3) Capable of producing a reset signal upon power on when external resistors and capacitors are used.

Pin configuration (top view)

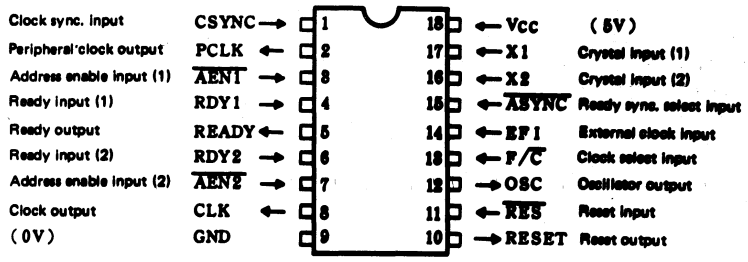


Fig. 13

Functional outline

The 8284 is a clock generator and driver designed exclusively for the 8086 processor. It contains a quartz-controlled oscillator, frequency divider (1/3) to create the clock output, frequency divider (1/2) to produce the peripheral clock output (PCLK), reset logic to synchronize with the CLK, and ready logic. The $\overline{RES}$ input accepts an external signal that is used to produce a CPU reset signal which is synchronous with the CLK output, and uses a Schmitt trigger circuit in its input. A power-on reset signal can be produced by connecting a resistor and capacitor to this $\overline{RES}$ terminal.

Block diagram

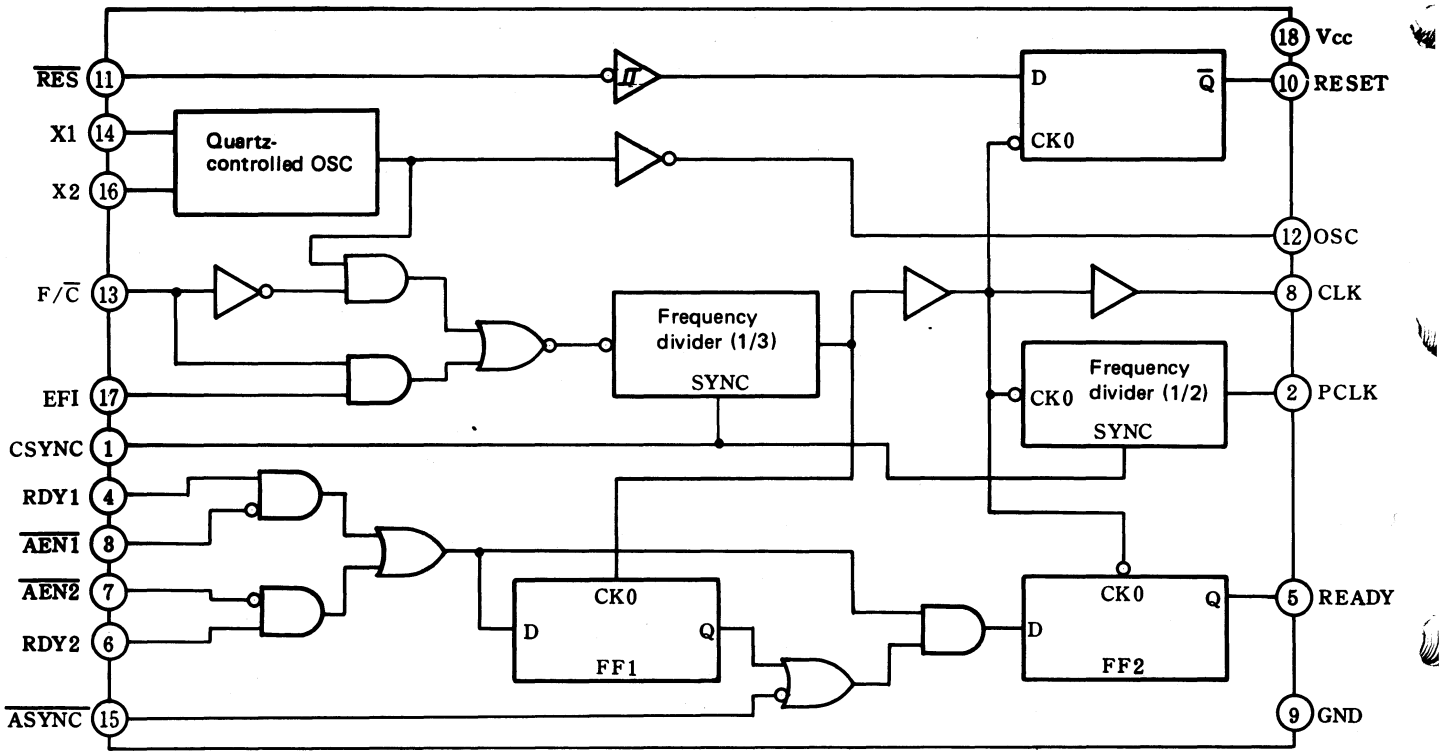


Fig. 14

4-4 8288 bus controller

Highlights

(1) Outputs with a large number of fan-outs.
(2) Advanced write control outputs ($\overline{AIOWC}$ and $\overline{AMWC}$)

Pin configuration

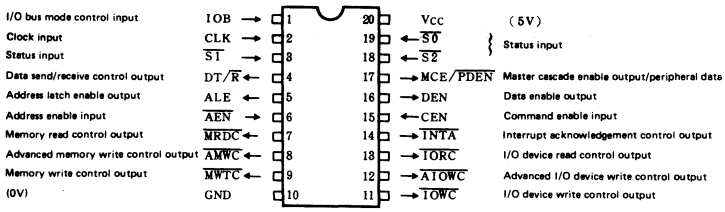


Fig. 15

Functional outline

The 8288 is a bus controller and driver used with the 8086 CPU operating in the maximum mode. It decodes the S0-S2 outputs from the CPU into command and control signals and provides control signals for I/O devices and memory. The 8288 is usable in the multi-master configuration in which more than one master CPU is attached to a single data bus. The 8288 has an input pin to accept the control signal $\overline{AEN}$ from the bus arbitor 8289.

Block diagram

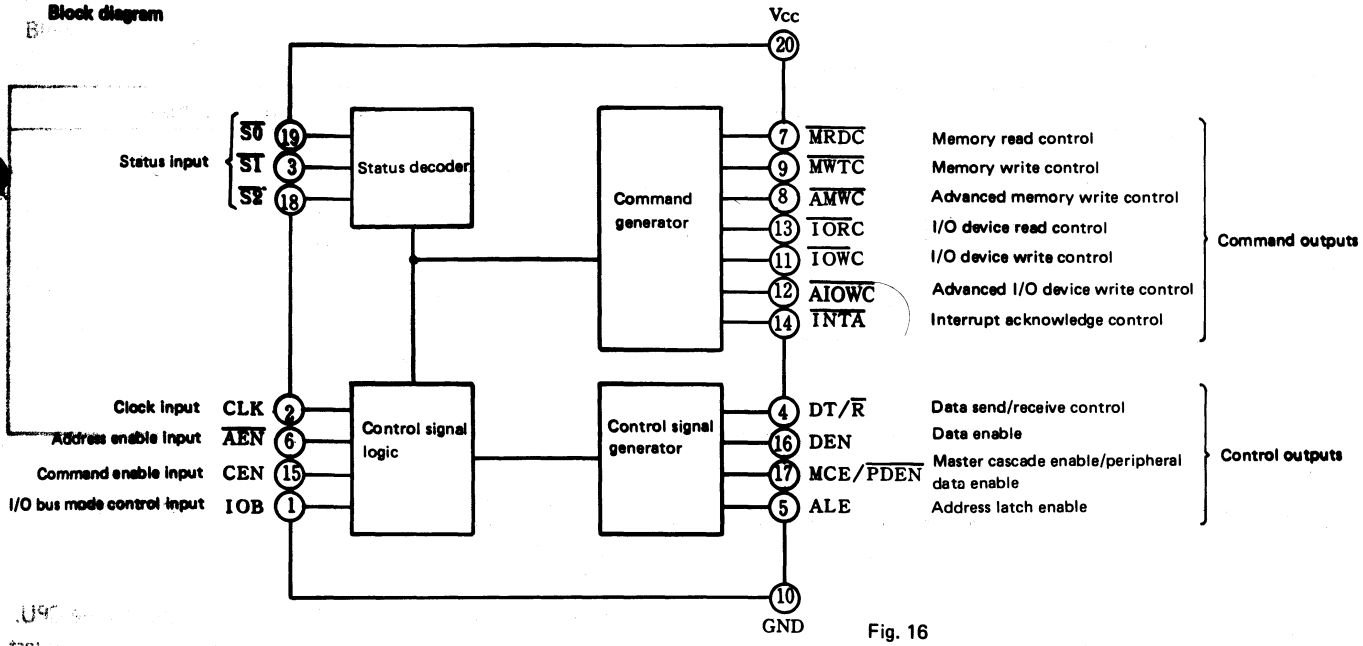


Fig. 16

Pin functions

Table 12

Pin No.	Pin name	Function	IN/OUT	Description
19,3,18	$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	Status input	IN	Accept each status output S0 – S2 from the CPU. The 8288 produces command and control signals from these input signals at the appropriate timings. Each of these pins has a pull-up resistor.
2	CLK	Clock input	IN	Accepts the clock output (CLK) of the clock generator 8284. The output timing of the 8288 varies with the clock rate applied to this pin.
5	ALE	Address latch enable output	OUT	Provides a strobe to the address latch. This pin is connected to the E pin of 74LS373 latch to latch address information from the CPU.
16	DEN	Data enable	OUT	Provides a data enable signal to the data bus transceivers on the local or system bus (active high).
4	DT/$\overline{R}$	Data transmit/ receive control output	OUT	Controls data flow between the CPU and memory or I/O devices. When this pin is high, the CPU is enabled to write data into a peripheral device; when it is low, the CPU is enabled to read data from the device.
6	$\overline{AEN}$	Address enable input	IN	If this pin is set high with the IOB input held at low, all the command outputs are placed in three-state logic. If the IOB input is high, this input causes the command outputs, other than $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$ and $\overline{INTA}$, to be placed in three-state logic.
15	CEN	Command enable input	IN	If this pin is set low, all the command outputs, DEN and $\overline{PDEN}$ control outputs are disabled (non-three-state logic). If it is set high, these outputs are enabled.
1	IOB	I/O bus mode control input	IN	If this pin is set high, the 8288 is placed in the I/O bus mode; if it is set low, the 8288 is placed in the system bus mode.
12	$\overline{AIOWC}$	Advanced I/O device write control output	OUT	Similar to the $\overline{IOWC}$, this pin functions as an I/O device write control output, but goes low one clock period in advance of the $\overline{IOWC}$. Active low output.
11	$\overline{IOWC}$	I/O device write control output	OUT	Active low output to command an I/O device to write the data onto the data bus.
13	$\overline{IORC}$	I/O device read control output	OUT	Active low output to command an I/O device to read the data onto the data bus.
8	$\overline{AMWC}$	Advanced memory write control output	OUT	Similar to the $\overline{MWTC}$, this pin functions as a memory write control output, bus goes low one clock period in advance to the $\overline{MWTC}$. Active low output.
9	$\overline{MWTC}$	Memory write control output	OUT	Active low output to command memory to write the data from the data bus.
7	$\overline{MRDC}$	Memory read control output	OUT	Active low output to command memory to output data onto the data bus.
14	$\overline{INTA}$	Interrupt acknowledge control output	OUT	Indicates interrupt acknowledge to the device in request for interrupt service, and commands the device to output the vector address onto the data bus. During an interrupt cycle, it functions the same way as the $\overline{IORC}$. Active low output.
17	MCE/$\overline{PDEN}$	NU	OUT	Master cascade enable or Peripheral data enable

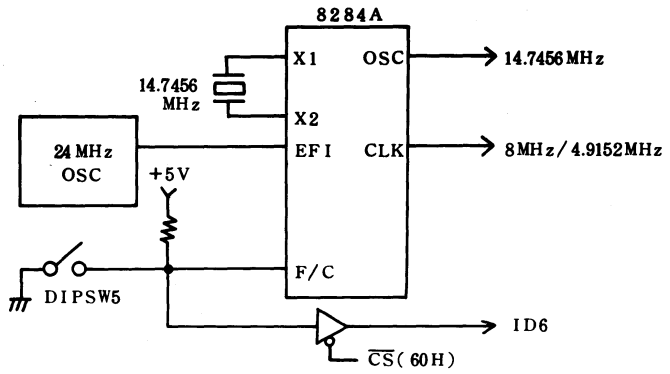
Status input versus command outputs

Table 13

S2	S1	S0	8086 status	Valid command output
L	L	L	Interrupt acknowledge	$\overline{INTA}$
L	L	H	Data read from I/O port	$\overline{IORC}$
L	H	L	Data write to I/O port	$\overline{IOWC}$ $\overline{AIOWC}$
L	H	H	Hold	–
H	L	L	Instruction fetch	$\overline{MRDC}$
H	L	H	Data read from memory	$\overline{MRDC}$
H	H	L	Data write into memory	$\overline{MWTC}$ $\overline{AMWC}$
H	H	H	Passive state	–

4-5 System clock

1. Block diagram



2. Operational description

The MZ-5600 runs under two modes of CPU clocks; the one under the high speed mode of 8 MHz and the other under the low speed mode of 4.9152 MHz, of which choice is made by means of the system switch 5.

When SW5 = ON: 4.9152 MHz

When SW5 = OFF: 8 MHz

Since the state of the SW5 is represented by the bit 6 of the input port (60H), it permits to identify the system clock.

4-6 8259A programmable interrupt controller

Highlights

(1) Single +5V power supply.

(2) Automatically produces a Interrupt vector to the CPU.

(3) Priority interrupt masks at each interrupt request terminal and vector address specification are all programmable.

(4) Controls up to 64 levels of interrupt requests by cascading the 8259.

(5) TTL compatible.

Pin configuration (top view)

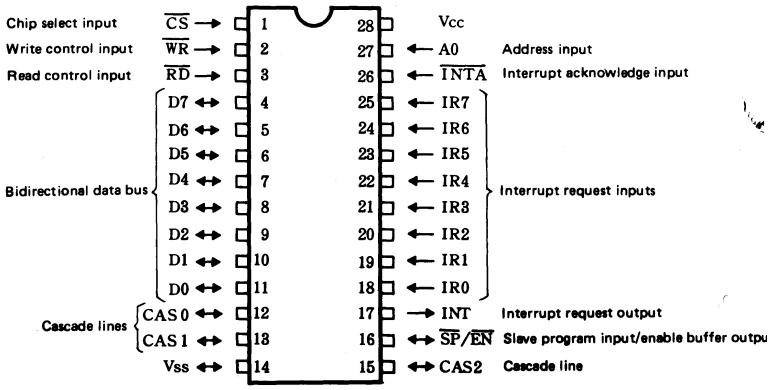


Fig. 17

Functional outline

The 8259A is an integral interrupt controller with eight levels of interrupt request input pins.

If an interrupt request arrives at one of the interrupt request pins of the 8259A, it identifies the mask condition and priority of the interrupt, then sends an INT signal to the CPU. The 8259A subsequently delivers the preprogrammed vector address onto the data bus in response to the INTA signal transferred from the system controller.

Block diagram

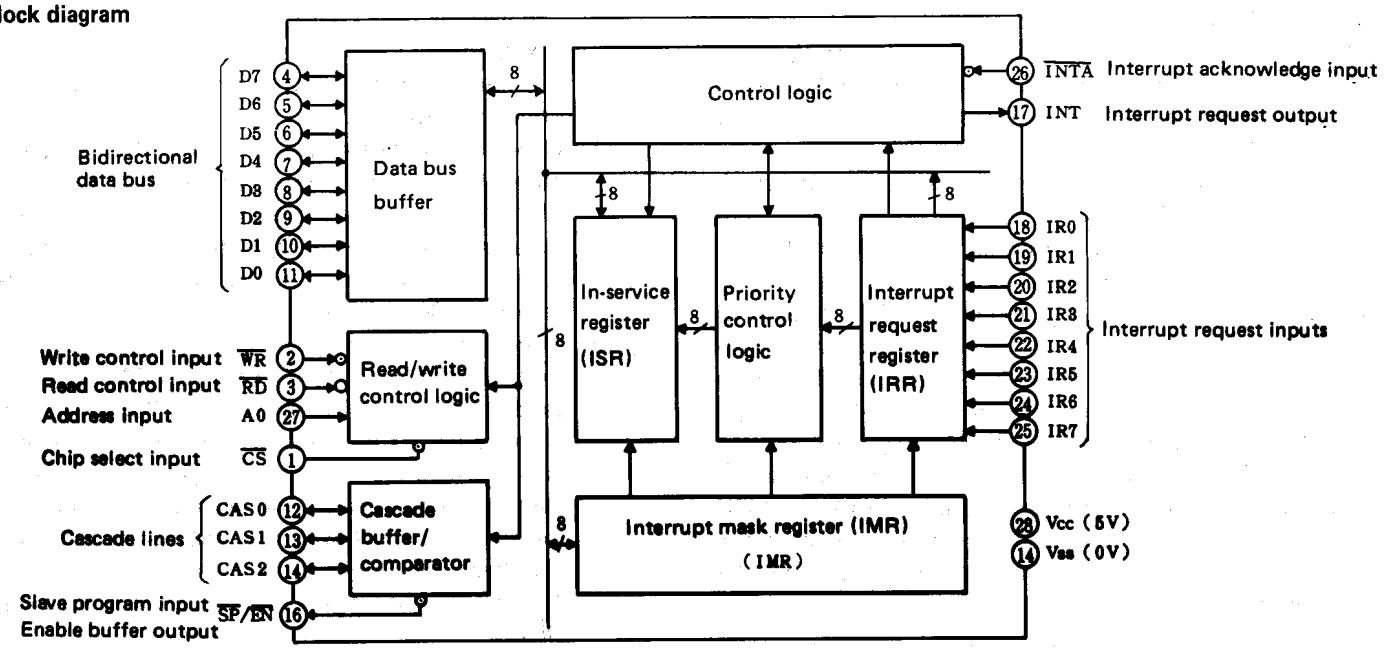


Fig. 18

Pin functions

Table 14

Pin No.	Pin Name	Function	IN/OUT	Description
1	$\overline{CS}$	Chip select input	IN	Active low input, but may be high during interrupt request input or interrupt service sequence.
2	$\overline{WR}$	Write control input	IN	Controls command write from the data bus.
3	$\overline{RD}$	Read control input	IN	Controls data read onto the data bus.
4~11	D7~D0	Bidirectional data bus	IN/OUT	All data and command transfers to or from the CPU is performed through this bidirectional bus.
12,13,15	CAS2~CAS0	Cascade lines	IN/OUT	These lines are output when addressed as a master, and are input when addressed as a slave. The master uses three-bit code to specify a slave via these cascade lines. The slave compares the code on the cascade lines with its own slave ID code. If agreement is found, it outputs data onto the data bus.
16	$\overline{SP}/\overline{EN}$	Slave program control input/ enable signal output	IN/OUT	In normal mode, $\overline{SP}/\overline{EN}$ = 1 specifies a master, and $\overline{SP}/\overline{EN}$ = 0 specifies a slave (SP). In the buffer mode, outputs a low level only if the data bus output is enabled ($\overline{EN}$).
17	INT	Interrupt request output	OUT	Outputs an INT signal to the CPU when an interrupt request arriving at one of the IR7 – IR0 inputs is acknowledged.
18~25	IR7~IR0	Interrupt request inputs	IN	Active high asynchronous interrupt request inputs (maskable). Order of priority can be altered. Each input has a pull-up resistor. For edge trigger operation, this input must be held high until the first $\overline{INTA}$ is received.
26	$\overline{INTA}$	Interrupt acknowledge input	IN	Accepts an interrupt acknowledge from the CPU. When an $\overline{INTA}$ pulse is received, the 8259 outputs a CALL command or vector address onto the data bus.
27	A0	Command/data control input	IN	Used in conjunction with the $\overline{WR}$ or $\overline{RD}$ signal to write commands or read status information. Normally connected to one of the address lines.

Interrupt sequence

(1) If an interrupt request pulse is applied to one or more of the interrupt request inputs (IR) of the 8259A, all the pertinent bits of the interrupt request register (IRR) will be set.

(2) If the interrupt request is not masked, the 8259 sends an INT signal to the CPU.

(3) Upon receipt of the INT signal, the CPU respons to it with an acknowledge signal $\overline{\text{INTA}}$.

(4) When receiving the first $\overline{\text{INTA}}$, the 8259 determines the order of priority. When it is functioning as a master, it outputs the number of the slave for which the interrupt was acknowledged, to its CAS pin.

(5) When receiving the second $\overline{\text{INTA}}$ from the CPU, the 8259 outputs an 8-bit interrupt vector address onto the data bus synchronized with the second $\overline{\text{INTA}}$. The CPU reads this vector address at the trailing edge of the $\overline{\text{INTA}}$, and jumps to the interrupt routine specified by the vector value.

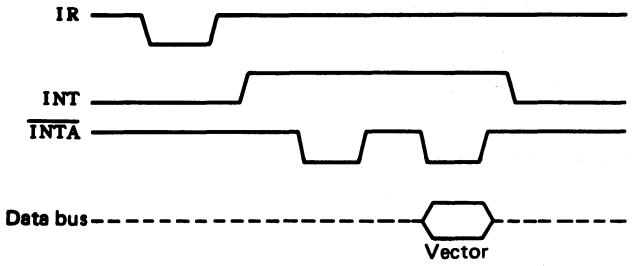
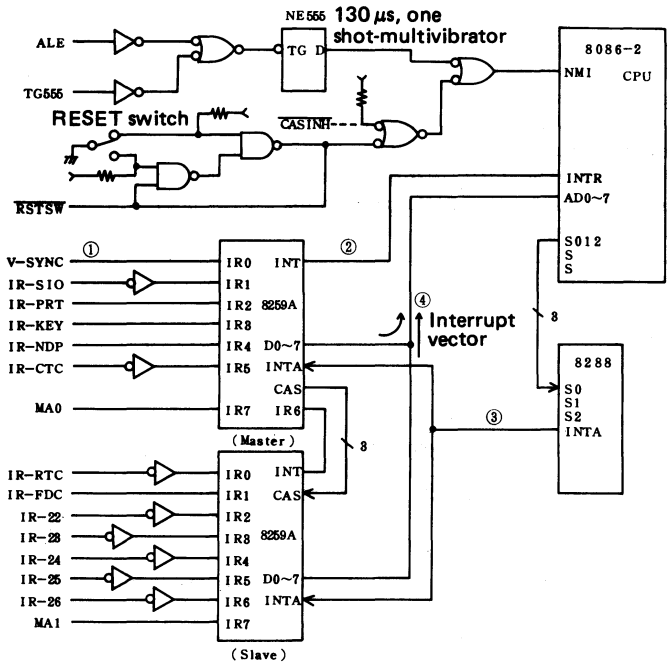


Fig. 19

4-7 Interrupt circuit

1. Block diagram



2. Operational description

1) Non-maskable interrupt to the CPU will arise under one of the following two (three) conditions.

a) Upon depression of the RESET switch located on the front side of the unit.

b) When tried to access a memory and I/O area not existing, but limited to the *$\overline{\text{XACK}}$ area on the map, in order to check an existence of a software bug or connection of the optional board.

c) With the SEEG version of the MZ-5600, when a certain task tried to access the memory area not permitted to access.

(1) When the software has run wild, the operation is normally halted by turning power off or resetting the CPU. With this model the program is reset by the software using NMI in order to retain the RAM, except for such a wild program run that may destroy the NMI vector or NMI routine.

(2) Since this unit is the system of normally non-ready, the ready signal is issued to the CPU or DMAC only when a valid memory or I/O is accessed. When an invalid memory or I/O is accessed, it makes the system as if halted. Therefore, if the ready signal has not returned within a certain period, the ready signal is issued from the timeout circuit which is sent to the CPU on the NMI line.

Theory of ready signal generation from the timeout circuit.

The one-shot multivibrator is triggered and its output is kept high by the ALE signal which is issued at the start of the bus cycle, when the CPU is continuing effective access, or by the TG555 signal which appears at the last stage of the DMA cycle or issued normally at every 13 μs for memory refresh, when a long internal processing such as multiplication is taken place. But, the one-shot multivibrator output is in low level when an invalid memory or I/O is accessed as it does not contain the ALE or TG555 signal.

As the state of the RESET switch can be sensed by means of the RSTSW signal which appears on the input port (60H, bit 1), the reset NMI can be discriminated from the timeout NMI.

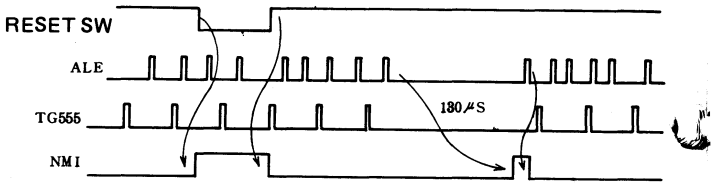
(3) See the section discussing protection.

2) As all interrupts are controlled by the 8259A except for NMI, request for interrupt is informed to the CPU after evaluating their priority.

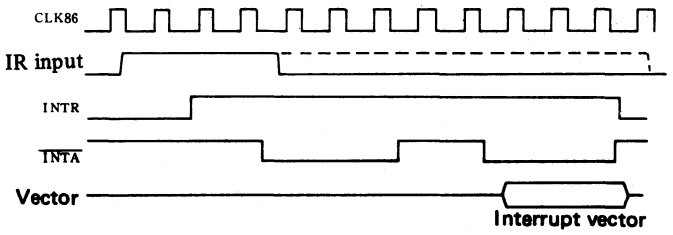
When there is an interrupt from a device by making the IR input of the 8259A high, it causes the INTR of the CPU to go high, if the IR input is not masked. If the CPU is ready for acception of interrupt, it makes the interrupt acknowledge cycle executed so that the 8288 returns the INTA signal to the 8259A. Upon receiving INTA, the 8259A sends on the data bus the vector corresponding to that interrupt request. As there are two INTAs, the interrupt request must be held until the first INTA. If not, the 8259A assumes the action as if IR7 is interrupted.

Timings

1) NMI



2) INTR



4-8 Bus control logic

(1) Block diagram

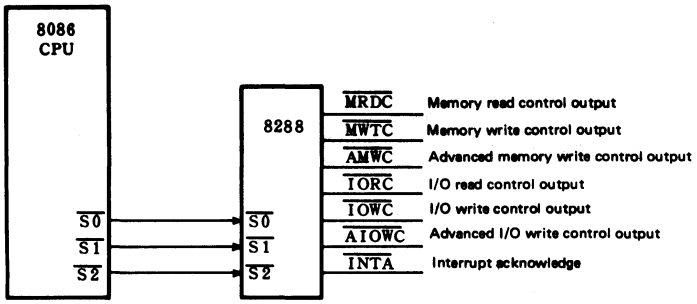


Fig. 22

(2) Description

When the 8086 is used in the maximum mode, commands (RD, WR, INTA) are output as status information (S0-S2), which are decoded by the 8288 to furnish control signals to memory and I/O devices.

(3) Timing chart

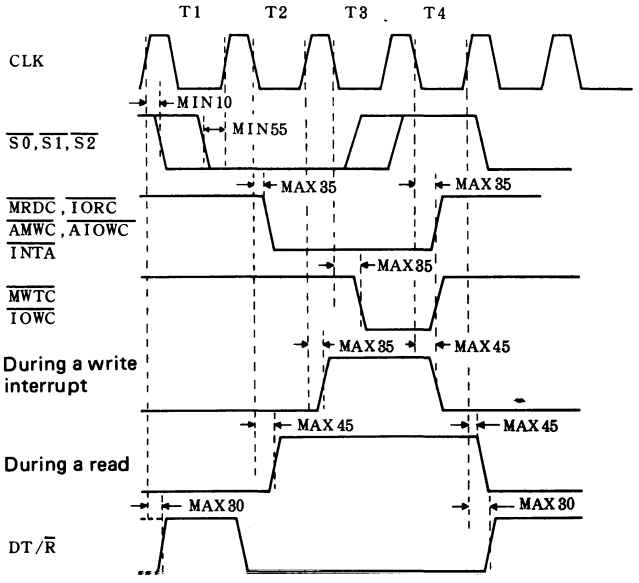
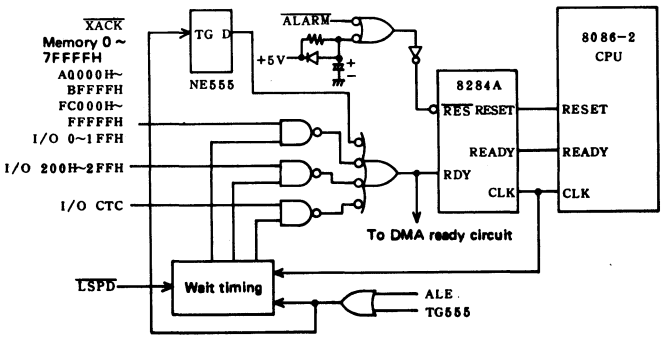


Fig. 23

4-9 Reset, ready circuit

1. Block diagram



2. Operational description

1) Reset

For reset of the 8086 CPU, the alarm signal from the power supply and the rising edge of +5V at the time of power on are detected by the CR time constant. The reset signal to the CPU is internally synchronized with the clock by the 8284A.

Refer to the section discussing the power supply unit for alarm timing.

2) Ready

Because the MZ-5600 employs the non-ready system, the ready signal is returned to the CPU only when access is valid. Though the memory or I/O decoder signal is actually supplied to the 8284A, it makes RDY signal delayed in synchronization with CLK in the WAIT timing circuit for a device that needs wait.

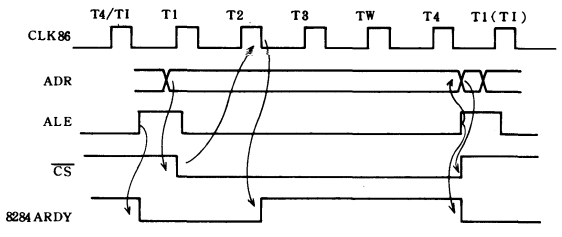
The ready signal is returned automatically from the timeout circuit when an I/O or memory in the XACK area is tried to access, to send NMI to the CPU.

See below for wait of each device.

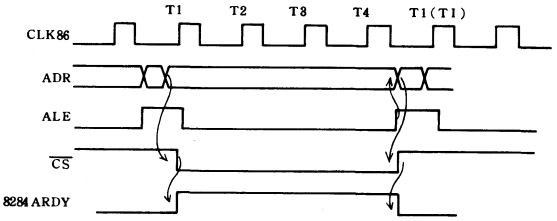
	8M mode	5M mode
○ System RAM ○ IPL ROM ○ Kanji/dictionary ROM ○ I/O other than below	1	0
○ SIO ○ RTC ○ PSG ○ PB	3	3
○ CTC ○ INTACK ○ INT RET	15	15
○ VRAM ○ I/O (380H~3FFH) ○ Memory other than above	XACK or 1	XACK

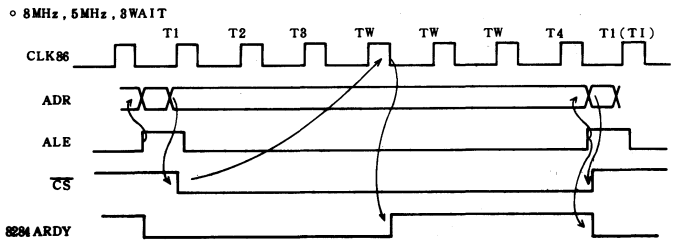
3. Timings chart

○ 8MHz 1WAIT

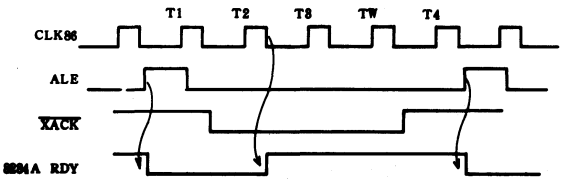


○ 5MHz 0WAIT

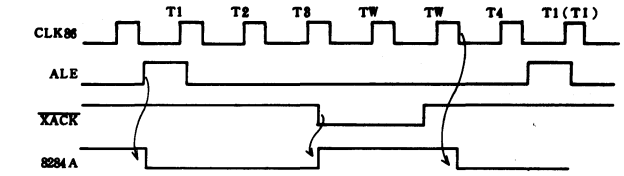




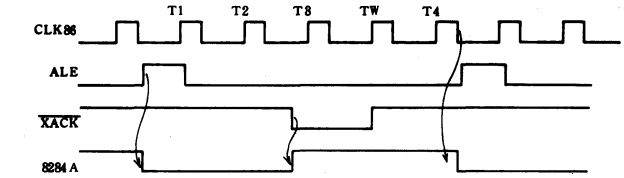
○ 8MHz XACK (In the case of XACK is 0 WAIT)



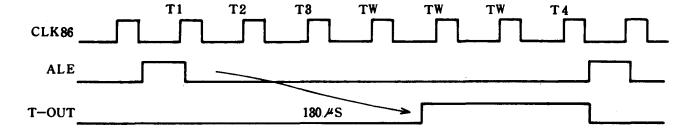
○ 8MHz XACK (In the case of XACK is 1 WAIT)



○ 5MHz XACK

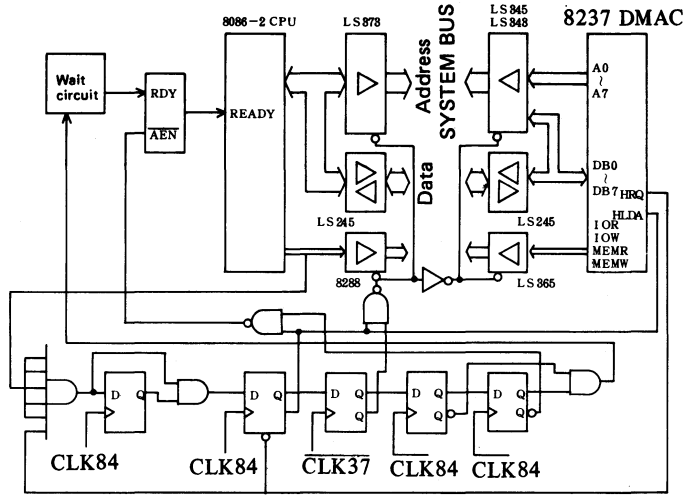


○ Time out ready



4-10. Hold conversion circuit

1. Block diagram



(1) When a DMA transfer request signal DREQ is issued to either of channels 0 through 3, the DMAC sends the hold request signal HRQ to the hold conversion circuit if that the channel is not masked.

(2) When in the CPU address cycle (*$\overline{S0}$, *$\overline{S1}$, *$\overline{S2}$, *$\overline{LOCK}$ are all "1") or during bus access, the hold conversion circuit returns to the DMAC the hold acknowledge signal HLDA at the final cycle (T4). And the CPU address bus, data bus, and command bus are isolated from the system bus to enable the DMA bus.

(3) At the same time, AEN of the 8284A is enabled to keep the CPU in the not ready condition. If the CPU should go into the next bus cycle, it awaits for returning of bus control while executing the wait cycle.

(4) DMA transfer is done under the control of the 8237A.

(5) As the DMAC releases HRQ upon completion of DMA transfer, the system bus is changed from the DMA bus to the CPU bus and the wait circuit is reset after enabling the 8284A again.

(6) The CPU executes the wait cycle on the local bus, but acts as if the bus cycle started from T1 on the system bus after reset of the wait circuit.

5. MEMORY CONTROL LOGIC

5-1 Chip selection

(1) Block diagram

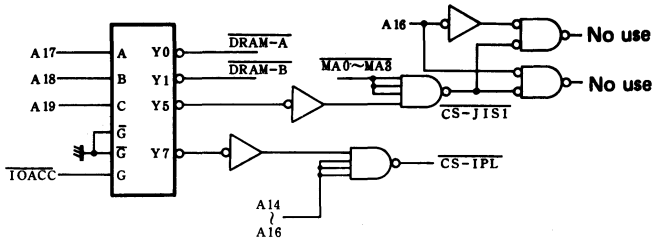


Fig. 26

(2) Description

If the $\overline{IOACC}$ signal is high, each ROM and RAM chip is selected. The following shows the relationship between the device address and the chip selected:

Dynamic RAM-0 = $\overline{A19}.\overline{A18}.\overline{A17}$
(00000H to 1FFFFH)

Dynamic RAM-1 = $\overline{A19}.\overline{A18}.A17$
(20000H to 3FFFFH)

CS-IPL = A19.A18.A17.A16.A15.A14
(FC000H to FFFFFH)

5-2 Address multiplexer

(1) Block diagram

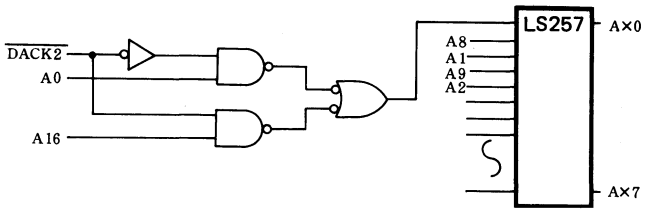


Fig. 27

(2) Description

The address multiplexer provides A1–A16 outputs when accessing the RAM, and A0–A15 when refreshing it. This is needed because the address viewed from

the CPU differs from that viewed from the DMA controller. Address switching occurs so that the refreshing specifications of 128 addresses/2ms is fulfilled.

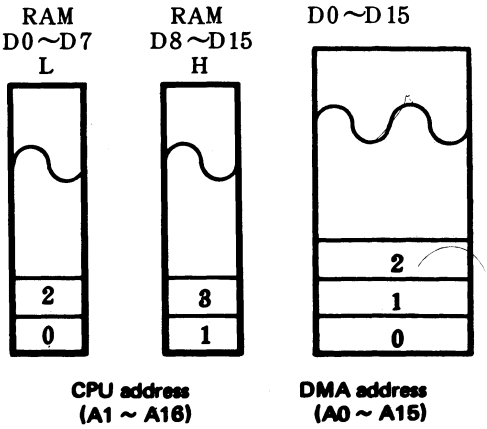


Fig. 28

5-3 Dynamic RAM read/write logic

(1) Block diagram

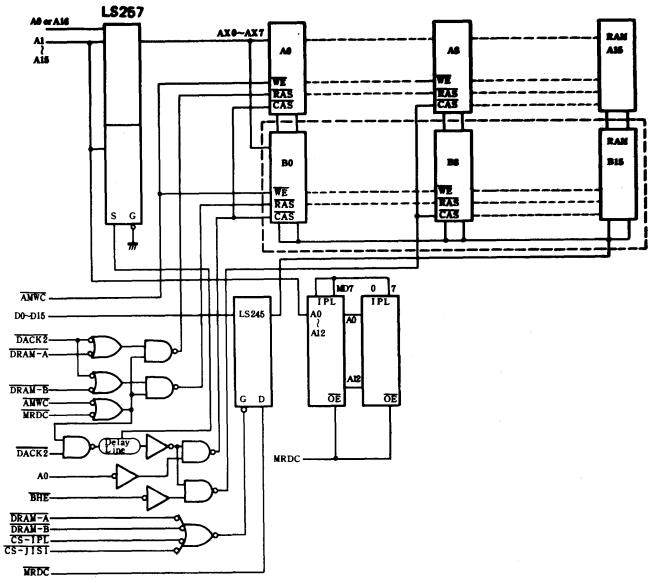


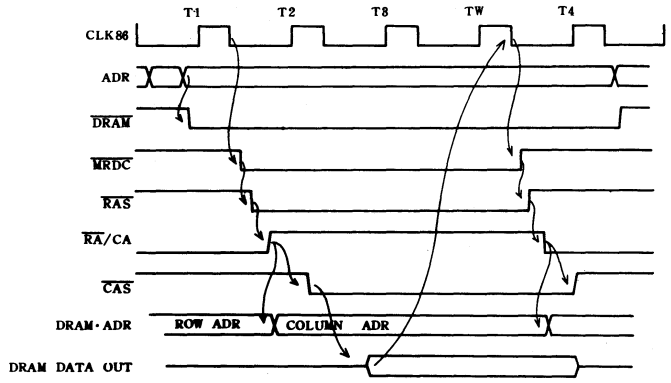
Fig. 29

(2) Description

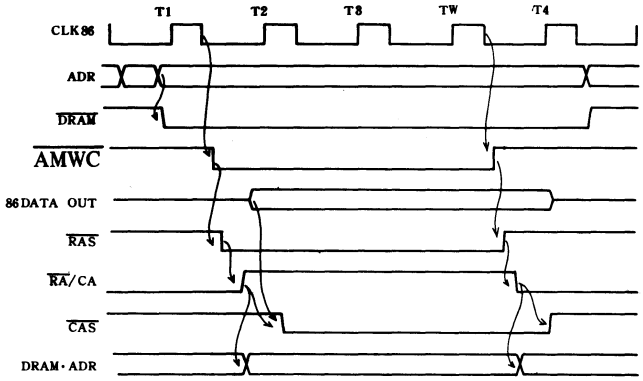
The $\overline{CAS}$ line uses a delay logic so that address is output 40ns after the $\overline{MRDC}$ or $\overline{AMWC}$ signal is output, and the $\overline{CAS}$ signal is output 70ns after address is output. The $\overline{DACK2}$ signal applied to the input gate of the delay logic is used to inhibit the CAS signal during refreshing. The $\overline{RAS}$ signal is output when the $\overline{DRAM}$-*, $\overline{MRDC}$, and $\overline{AMWC}$ signals are all active. The $\overline{DACK2}$ is used to output the $\overline{RAS}$ signal during refresh regardless of the chip select signals. ($\overline{DRAM}$-*).

(3) Dynamic RAM read/write timing

○ 8MHz Read cycle



○ 8MHz Write cycle



5-4 Dynamic RAM refresh

(1) Description of operation

Unlike the Z80, the 8086 has no refreshing logic. On the MZ-5600 system, dynamic RAM refreshing is accomplished by executing direct memory access (DMA) from memory to I/O at a certain interval.

(2) Timing chart

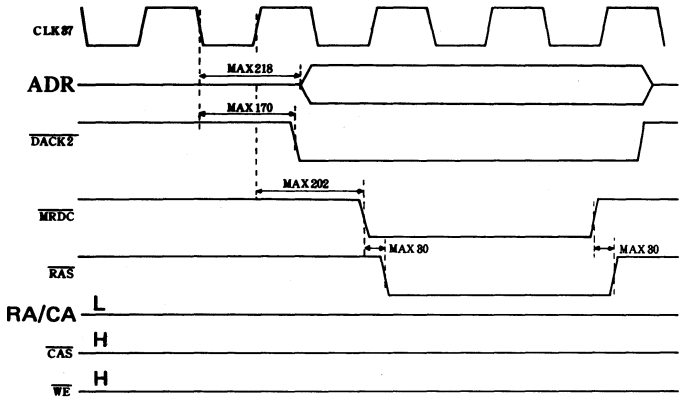


Fig. 31

(3) Description

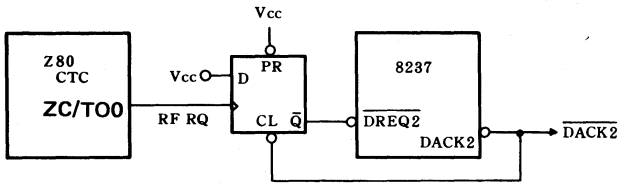


Fig. 32

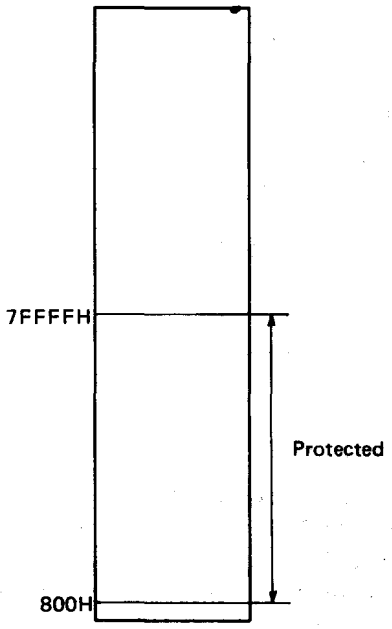
Channel 0 of the Z80CTC is used in the timer mode, and its output (ZC/TO0): Pulse with a 13μs period) is applied to the Data Request DREQ2 pin of the 8237 (DMA controller) via a type-D F/F as a refresh request signal. When receiving a DREQ2 signal, the 8237 outputs a Data Acknowledgement DACK2 to place itself in the DMA mode (see DMA interface).

5-5 Memory protection logic (MPL) [Used only SEEG]

Specification

1. Addresses protected

The IPL ROM, VRAM, vector RAM, and bank 1 are not protected.

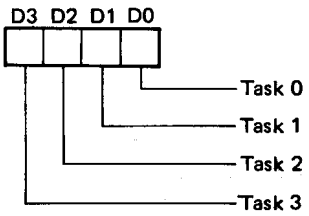


Since the bank 1 is for memory protection by itself, the protect function does not cover this area.

2. Task register

Since MPL is capable of managing four tasks, choice of task must be done in the following manner:

I/O address
60H
(Write only)



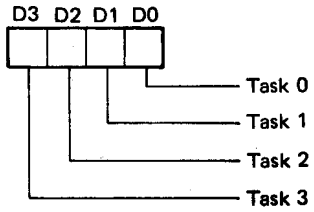
EX) 0001 → Task 0 in execution
0100 → Task 1 in execution

3. Protection memory

Depending on the nature of the task, read and write to the task is limited.

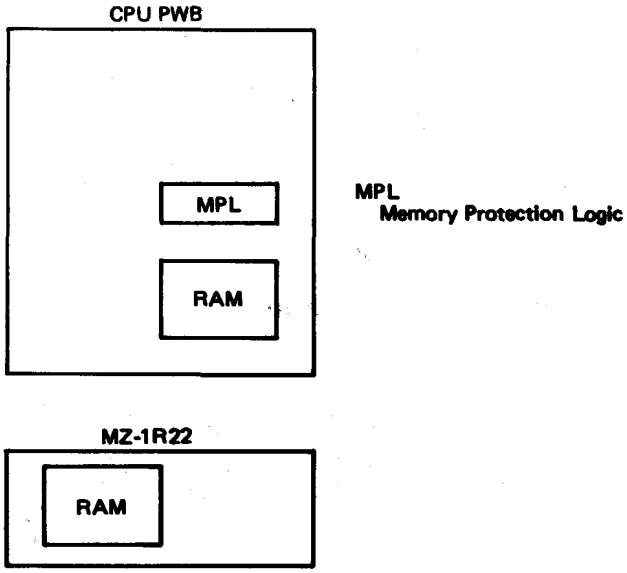
Memory address

BANK1 800H ~ 7FFFFH

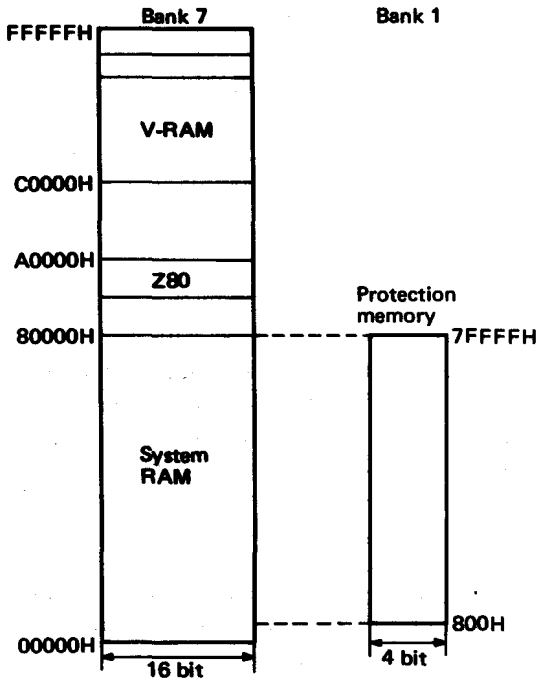


EX) 1101 → Only the task 0 is applicable
0011 → Tasks 2 and 3 are applicable

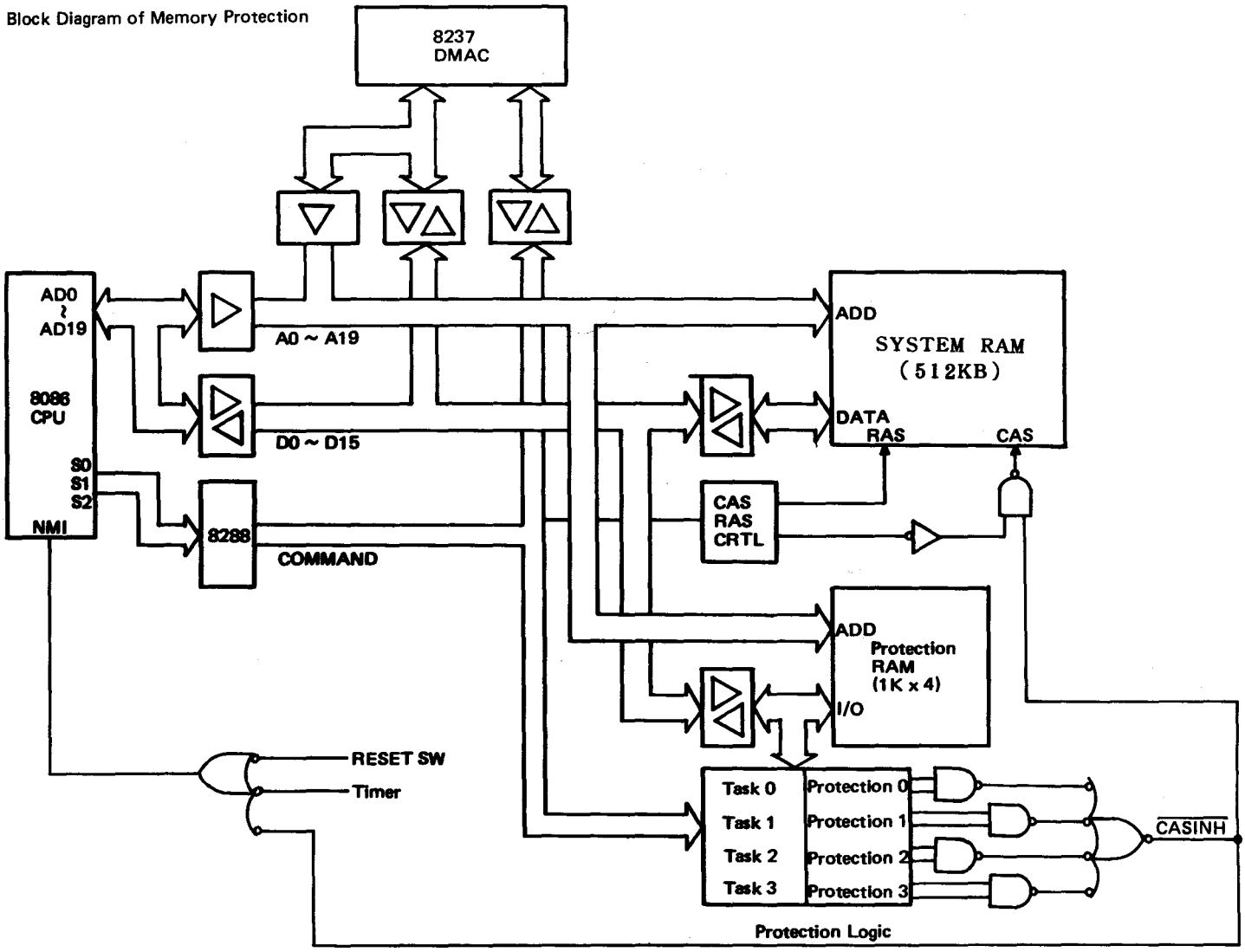
Location



Memory map



Block Diagram of Memory Protection



MPL operation

When four tasks are operated simultaneously in the time shared mode, every task is allocated to the system RAM area (512 KB, max.). If a task should try to access the system RAM beyond the limit, not only the RAM is protected, but also the condition is sensed and informed to the CPU with NMI.

Since the currently operating task is set in the task register (output on i/o address 60H), the task information should be set by the OS each time the task changes.

One word (4 bits) of the protection memory corresponds to one kilobytes of the system RAM, which is used to indicate the system RAM area the task can access. To enable the use of the 1 KB area of 54400H through 547FFH for the tasks 1 and 2 and to disable tasks 0 and 3, for instance, "1001" has to be set in the protect memory. MPL does not function at power on and when "0" is set in the task register.

Shown next is the procedure to set up the protection memory area.

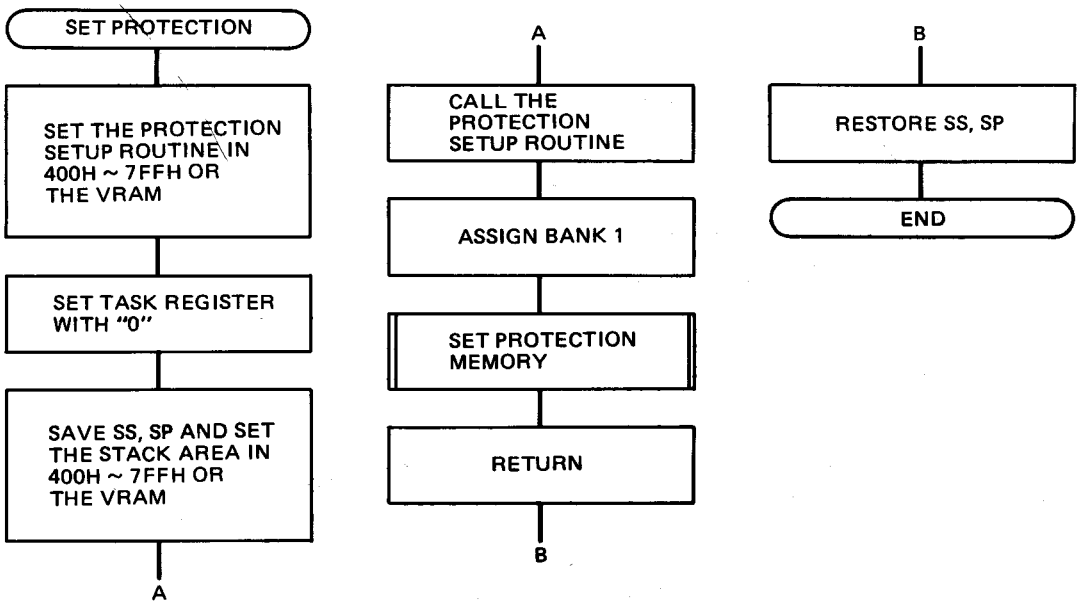
Theory of memory protection

For instance, the protection RAM area 10000H of the bank 1 contains "1010" to enable the 1 KB area of the system RAM 1000H – 103FFH for access by tasks 0 and 2. If the system RAM area of 1000H ~ 103FFH is tried to read or write during the execution of the task 1 with "0010" in the task register, the data "1010" is sent from the protection RAM. Then, the protection data "1010" is Ored with "0010" of the task register by the protection logic. Since the result would not be "0000" but "0010", it prohibits $\overline{CAS}$ signal from the system RAM. For the dynamic RAM, the same cycle as the RAS only fresh is executed, which in consequence disables to read or write to the RAM. At the same time, the NMI is issued to the CPU with the CAS inhibit signal.

The reason why $\overline{CAS}$ is prohibited for protection of the memory is that it is not practically possible to use a high speed protection RAM and the protection logic which are required to disable the read or write command using the address information.

WAVEFORMS

*1: The protection data are sampled at a high to low transition of the command and the contents of the task register is operated and CASINH is forced active if required. CAS would not go active as long as CASINH is active.



6. I/O DECODER LOGIC

6-1 Block diagram

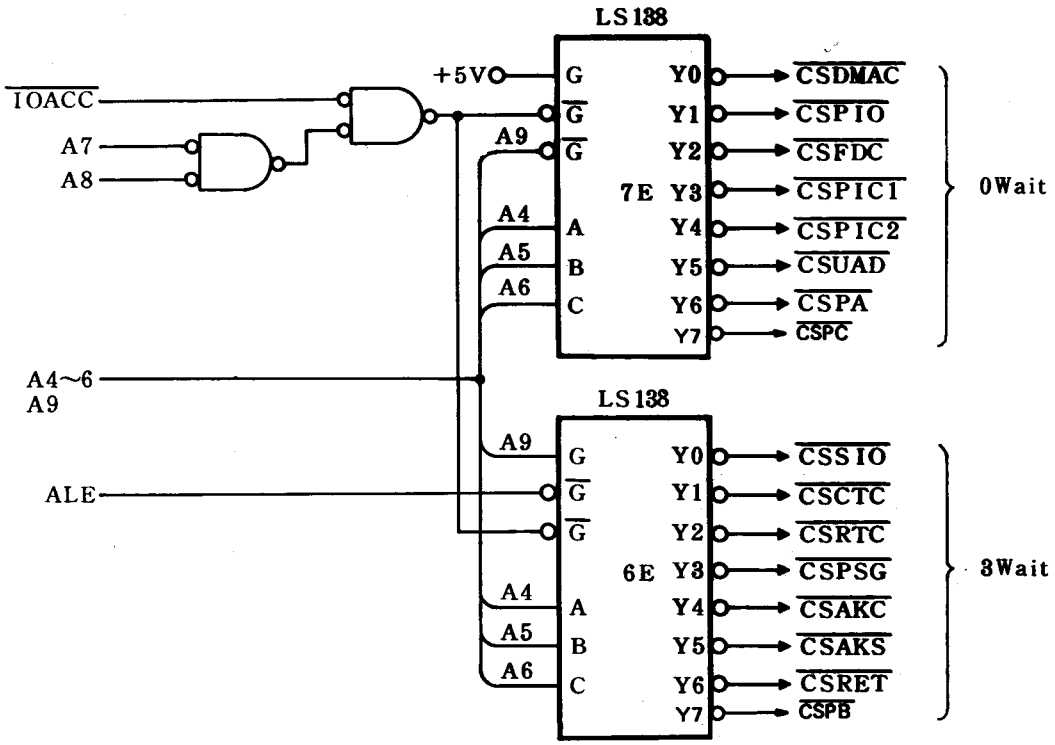


Fig. 33

As shown in the above figure, two integral decoders LS138's are used to provide chip selection for each I/O device on the CPU board.

6-2 I/O address map

Table 15

	HEX	15 – 12	11	10	9	8	7	6	5	4	3	2	1	0	DEVICE		WAIT
System PWB	00– 0F	X – X	X	X	0	0	0	0	0	0	A3	A2	A1	A0	DMAC (8237)	ID0-7	Byte Access
	10– 1F				0	0	0	0	0	1	X	X	A1	A0	PIO (8255A)	ID0-7	
	20– 2F				0	0	0	0	1	0	X	X	X	A0	FDC (μPD765)	1D0-7	
	30– 3F				0	0	0	0	1	1	X	X	A1	0	PIC1 (8259A) MASTER	AD0-7	
	40– 4F				0	0	0	1	0	0	X	X	A1	0	PIC2 (8259A) SLAVE	AD0-7	
	50– 5F				0	0	0	1	0	1	X	X	X	X	DMAC high-order address latch	ID4-7	
	60– 6F				0	0	0	1	1	0	X	X	X	X	PORT-A	ID0-7	
	70– 7F	X – X	X	X	0	0	0	1	1	1	X	X	X	X	PORT-C	ID0-3	
I/O slot	80– 8F	X – X	X	X	0	0	1	0	0	0	X	X	A1	A0	Reserved	ID0-3	
	F8– FF	X – X	X	X	0	0	1	1	1	1	1	A2	A1	A0	Reserved		
CRT PWB	100–10F	X – X	X	X	0	1	0	0	0	0	X	X	A1	0	GDC (μPD7220)	D0-7	0 Wait/ 5MHz 1 Wait/ 8MHz
	110–11F				0	1	0	0	0	1	X	X	A1	0	WDC (T)	D0-7	
	120–12F				0	1	0	0	1	0	A3	A2	A1	0	VDC2 (H2)	D0-2	
	130–13F				0	1	0	0	1	1	X	X	X	0	VDC1 (H1)	D0-2	
	140–14F				0	1	0	1	0	0	X	A2	A1	1	RFL I	D8-10	
	150–15F				0	1	0	1	0	1	X	A2	A1	1	RFL II	D8-10	
	160–16F				0	1	0	1	1	0	X	X	X	1			
	170–17F	X – X	X	X	0	1	0	1	1	1							
I/O slot	180–18F	X – X	X	X	0	1	1	0	0	0	X	A2	A1	0	Note		
	190–19F				0	1	1	0	0	1	X	A2	A1	0	Note	User area	
	1A0–1AF				0	1	1	0	1	0	X	X	X	X	Note		
	1B0–1BF				0	1	1	0	1	1					Note		
	1C0 –1FF	X – X	X	X	0	1	1	1	1	1	X	X	X	X	Reserved		
CPU PWB	200–20F	X – X	X	X	1	0	0	0	0	0	X	X	A1	A0	SIO (LH0084A)	1D0-7	Byte Access
	210–21F				1	0	0	0	0	1	X	X	A1	A0	CTC (Z-80CTC)	1D0-7	
	220–22F				1	0	0	0	1	0	A3	A2	A1	A0	RTC (PR5C01)	ID0-7	
	230–23F				1	0	0	0	1	1	X	X	X	X	PSG (AY-3-8198)	ID0-3	
	240–24F				1	0	0	1	0	0	X	X	X	X	CTC INT Reset	X	
	250–25F				1	0	0	1	0	1	X	X	X	X	SIO INT Reset	X	
	260–26F				1	0	0	1	1	0	X	X	X	X	CTC Return INT	ID0-7	
	270–27F	X – X	X	X	1	0	0	1	1	1	X	X	X	X	PORT-B	1D0-3	
I/O slot	280– 2FF	X – X	X	X	1	0	1	0	0	0					Reserved		3 Wait
	300– 340–	X – X	X	X	1	1	0	0	0	0					User area		
							0	1	0	0							
	37F	X – X	X	X	1	1	0	1	1	1					Reserved		
	380 –3BF –3FF	X – X	X	X	1	1	1	0	0	0					Reserved For I/O slot Not Ready generates within the System Unit. User area		X ACK

Note: 180H to 1BFH: PWB checker

X: Not in Decode

D0-15 – 16 Bit system BUS
ID0-8 – 8 Bit I/O BUS

6-3 I/O bit map

(1) System board

Table 16

DEVICE	ADD	BIT	SIGNAL NAME	I/O		AFTER P/O	INITIAL DEFAULT
8255 [Group A, Mode 1 / Group B Mode 0]	010H	PA0	$\overline{\text{DATA1}}$	OUT	Data output to Centronics I/F (negative polarity). Null codes are hex FF.	Input mode (FFH)	Output mode (FFH)
		PA1	$\overline{\text{DATA2}}$				
		PA2	$\overline{\text{DATA3}}$				
		PA3	$\overline{\text{DATA4}}$				
		PA4	$\overline{\text{DATA5}}$				
		PA5	$\overline{\text{DATA6}}$				
		PA6	$\overline{\text{DATA7}}$				
		PA7	$\overline{\text{DATA8}}$				
	011H	PB0	$\overline{\text{BUSY}}$	IN	Centronics I/F busy (busy if zero.)	Mode input	Mode input
		PB1	$\overline{\text{PE}}$		Centronics I/F.		
		PB2	PDTR		Centronics I/F select signal (selects if one.)		
		PB3	DK		Data bit from keyboard } Key		
		PB4	SRK		Output requested from keyboard } Key		
		PB5	$\overline{\text{CD}}$		Called signal } BSC transmission		
		PB6	$\overline{\text{CI}}$		Carrier sense } BSC transmission		
		PB7	MOTOR ON		MFD motor on status input		
	012H (013H)	PC0	DC	OUT	Data bit to keyboard }	Input mode (FFH)	1
		PC1	STC	OUT	Strobe to keyboard }		0
		PC2	$\overline{\text{EXCLK EN}}$	OUT	BSC external clock (BSC if High)		0
		PC3	IR-PRT	OUT	Interrupt by ACK input to Centronics I/F.		0
		PC4					0
		PC5	$\overline{\text{STROBE}}$	OUT	Centronics I/F $\overline{\text{STROBE}}$ output (⌐L⌐)		1
		PC6	$\overline{\text{ACK}}$	IN	Centronics I/F $\overline{\text{ACK}}$ input		X
		PC7		OUT	Not used.		X

NOTES:
1) Group A is used in Mode 1.
2) Group B is used in Mode 0.
3) The desired bit of the output to Group C may be set or reset using the control register (013H).
4) The bit PC6 is an interrupt enable flag (INTE), and is set or reset by the CPU.
5) While the $\overline{\text{ACK}}$ may be read by PC3, is needs not be read as its status is known to the CPU via the PIC.

Table 17

DEVICE	ADD	BIT	SIGNAL NAME	I/O		AFTER P/O	INITIAL DEFAULT
AY-3-8912 (Sound IC)	230H			OUT		Input mode (FFH)	0
							0
							0
							0
		IOA4	$\overline{\text{MOTOR ON}}$		Drive motor on signal (on if Low.)		1
		IOA5	MA0		} Area (A0000H~BFFFFH) bank select signal		0
		IOA6	MA1				0
		IOA7	MA2				
PORT-A (LS541)	060H	ID0	$\overline{\text{High Den}}$	IN	RESET switch input (on if zero) ← MFD selection	Input mode	Input mode
		ID1	$\overline{\text{RSTSW}}$				
		ID2	DIP SW1		SW1 } System DIP switches (see next page)		
		ID3	DIP SW2		SW2		
		ID4	DIP SW3		SW3		
		ID5	DIP SW4		SW4		
		ID6	DIP SW5		SW5		
		ID7	DIP SW6		SW6		

(1) When accessing the I/O port of the AY-3-8912 sound IC), load I/O register address into 231H, then write the I/O data to 230H.

(2) When initializing the IOA port, write the data to be output (described above), then place the port in the output mode. This is needed to maintain the SEL and MOTOR ON signals inactive during initialization.

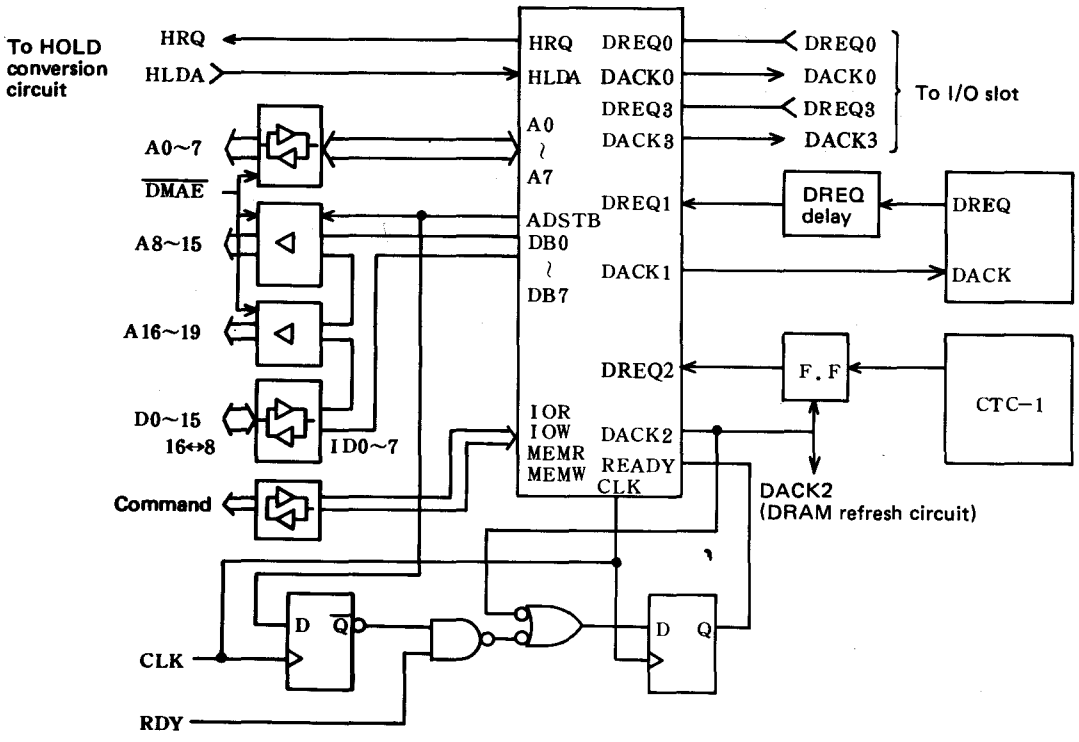
DEVICE	ADD	BIT	Signal name	I/O		After power on	Initialize
PORT-C (LS74)	070H	ID0		OUT		Don't care	
		ID1					
		ID2	High Den		MFD *1M/640K alternate signal		
		ID3	FDCRST		FDC reset signal (reset with "1")		
PORT-B (LS367)	270H	ID0		IN	("0" – SW OFF "1" – SW ON & CPU)	Input mode	
		ID1					
		ID2	DIP SW7		SW7 } System DIP SW (See separate page)		
		ID3	DIP SW8		SW8 }		

System dip switch function

		Function	Factory setup
SW1	OFF	For use of the high resolution display (400 reasters)	
	ON	For use of the middle resolution display (200 resters)	
SW2	OFF	Normally OFF	
	ON	Self-check mode*	
SW3		Reserved	
SW4			
SW5	OFF	8MHz CPU clock	
	ON	5MHz CPU clock	
SW6	OFF	8087 arithmetic processor not in use**	
	ON	8087 arithmetic processor in use	
SW7			
SW8			

7. DMA INTERFACE CIRCUIT

7-1 Block diagram

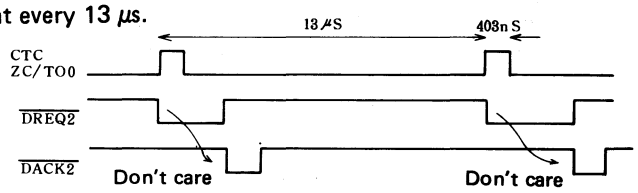


7-2 Operational description

As the 8237A programmable DMA controller is used, it has four independent DMA channels. Channels 0 and 3 are open for I/O slots; the channel 0 is dedicated for interface with the hard disk, and the channel 3 is for interface with the SFD.

Channel 1 is for interface with the standard MFD and is provided with the DREQ delay circuit of 5 x 4 MHz clock cycles in order to meet performance of DRQ through IORD of the FDC.

Channel 2 is for refresh of the system RAM which is done by reading the DRAM with the request from the CTC given at every 13 μs.

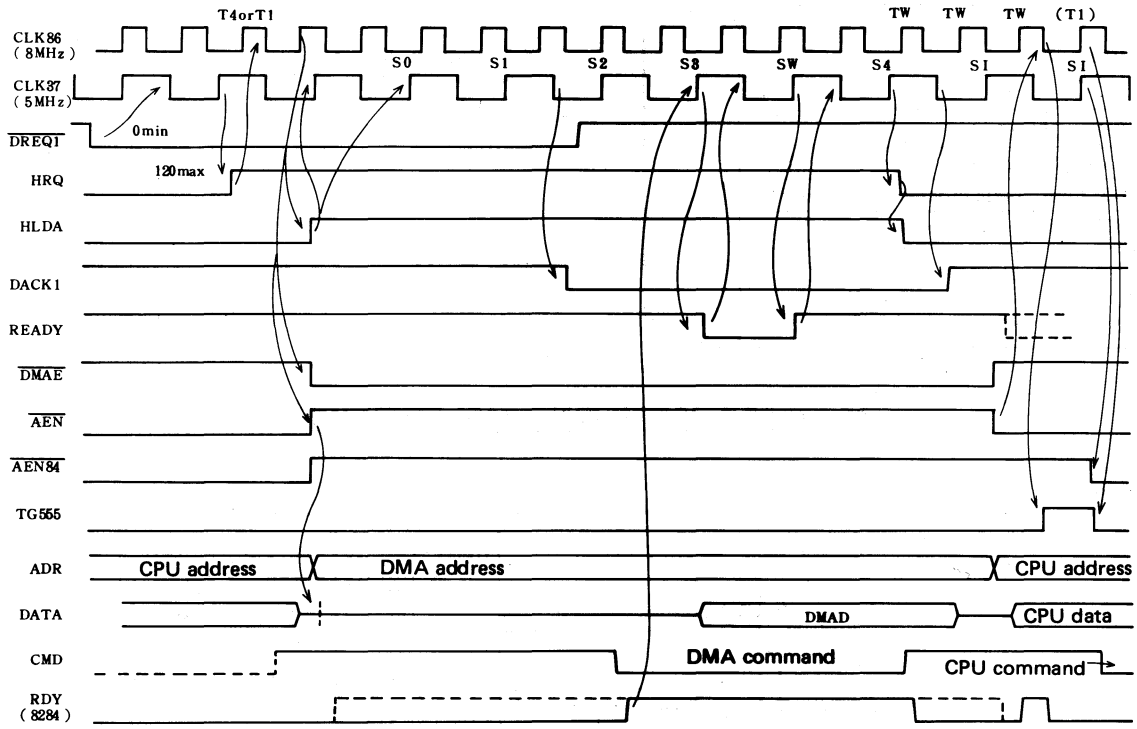


When DREQ appears on a channel, the DMAC issues the hold request signal HRQ to the CPU. When the hold conversion circuit receives this signal, it puts the CPU into the non ready state to open the system bus. At the same time, the hold acknowledge signal HLDA and DMA enable signal DMAE are returned to the DMAC to start DMA transfer. With the 8237 DMAC it is possible to control DMA transfer of 16 bits in total (64 KB); A0 ~ A7 issued by the DMAC itself and A8 ~ A15 which DB0 ~ 7 are latched by ADSTB at the start of the DMA transfer. To cover memory address space of 1 MB of the 8086 CPU, ID4-7 I/O (50H) latch signals are used as A16 ~ A19.

The DMAC goes ready with the DMA transferred memory ready signal, and one WAIT is attached automatically to the ready signal returned without a wait.

7-3 Timings

In the case of the DMA channel 1 (SW is not used for the channel 2)



* The CPU clock (CLK86) is not in complete synchronization with the DMA clock (CLK37).

7-4 μPD8237A DMA controller

(1) Highlights

1) Independent DMA-request enable/disable control.
2) Four independent DMA channels.
3) Automatically initializes individual channels.
4) Memory-to-memory transfer capability. (Not used for MZ5600)
5) Memory block initialization.
6) Address increment/decrement.
7) Transfer rate of up to 1.6MB/s. (2.5MB for compressed timing).
8) Can be expanded directly to any number of channels.
9) $\overline{EOP}$ input for termination of transfer.
10) Software DMA request.
11) Variable active levels on DREQ and DACK signal lines.

(2) Pin configuration

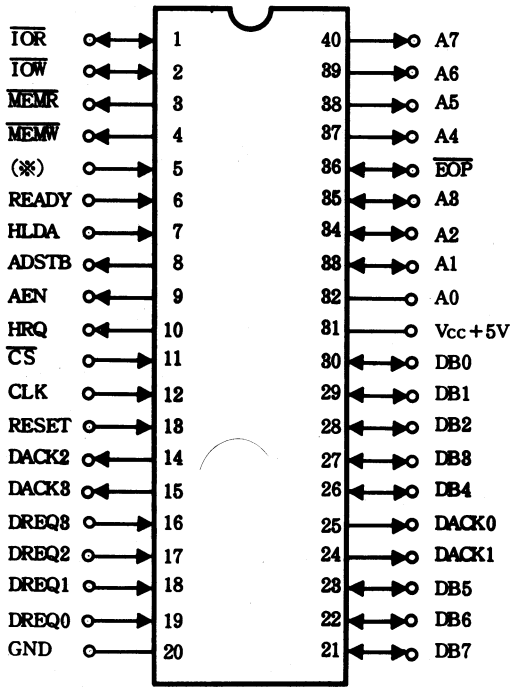
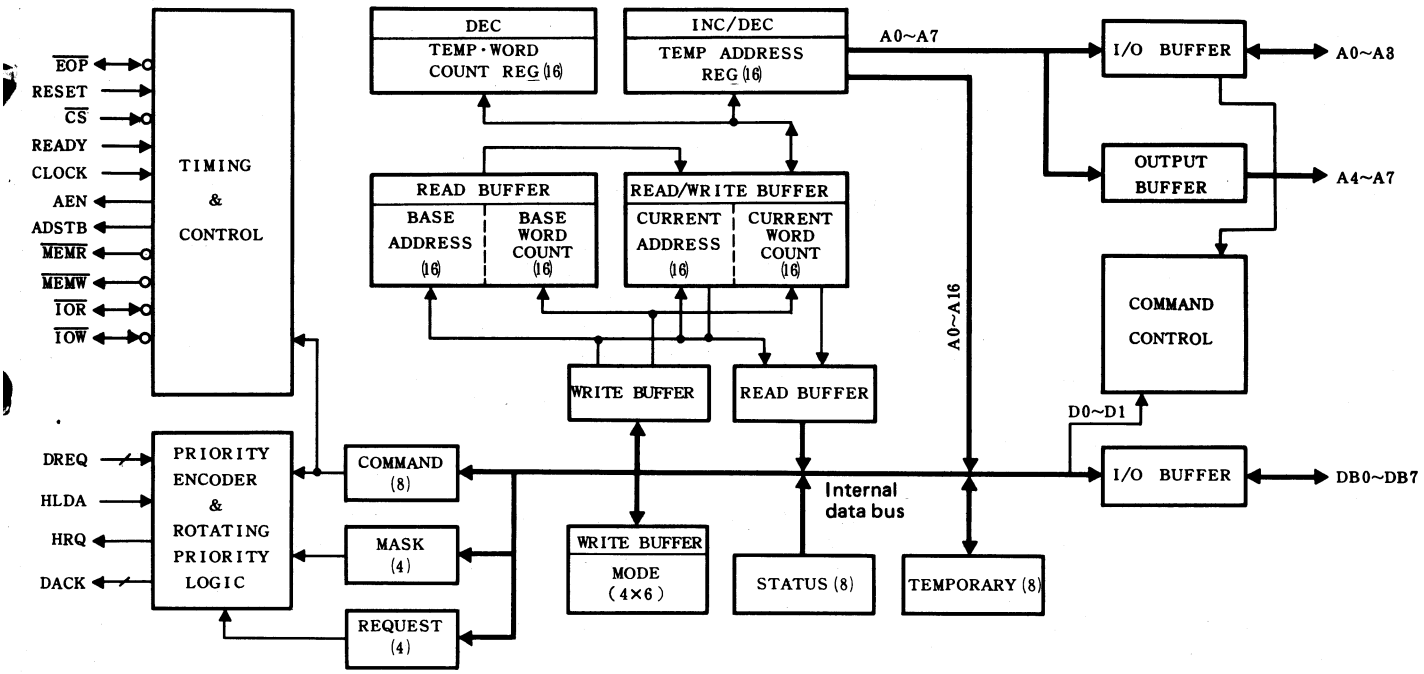


Fig. 38

(3) Block diagram

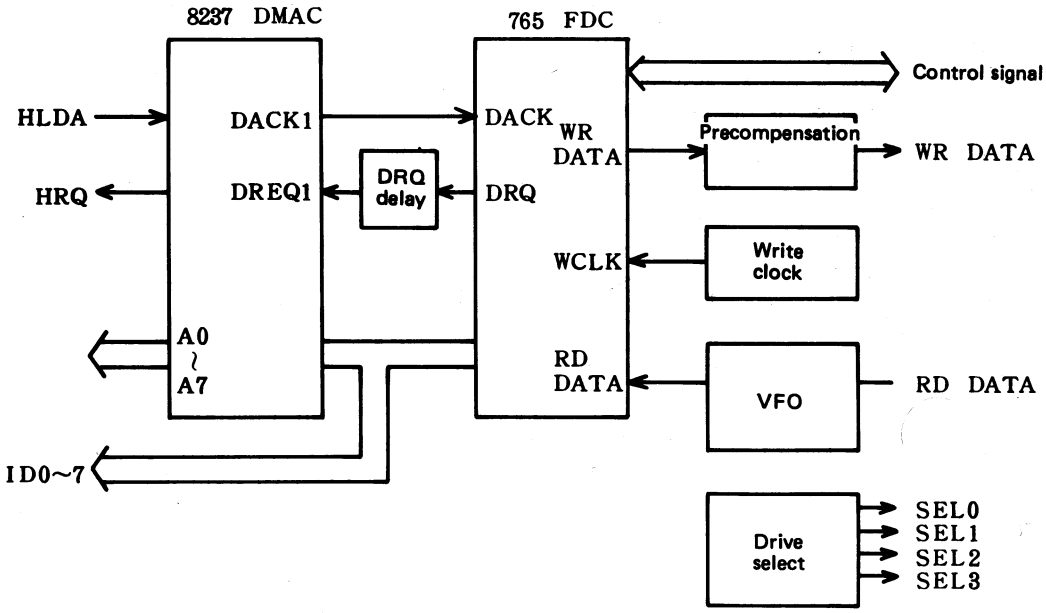


(4) Pin functions

Pin No.	Signal name	I/O	Description
1	$\overline{IOR}$	I/O	In idle cycles, the CPU uses this signal as an input control to read the control register. In active cycles, this signal is used as an output control signal with which the 8237A accesses data from peripheral logics during DMA write operations.
2	$\overline{IOW}$	I/O	In idle cycles, the CPU uses this signal as an input control to load information into the 8237A. In active cycles, the 8237A uses it as an output control to load data into peripheral logics during DMA read operations.
3	$\overline{MEMR}$	OUT	Used to access data from selected memory locations during DMA read. (active low, three-state output).
4	$\overline{MEMW}$	OUT	Active low, three-state output used to write data into the selected memory locations during DMA write.
5	(*)	IN	This input must always be held high.
6	READY	IN	Used to extend the memory read/write pulse width (which is output by the 8237A) so as to accommodate low-speed memory or I/O devices.
7	HLDA	IN	Active high hold acknowledge signal sent from the CPU, indicating the CPU has relinquished system bus access authority.
8	ADSTB	OUT	Active high address strobe used to strobe the high order address byte.
9	AEN	OUT	Used to enable the output of the latch holding the high-order 8 address bits, to output them onto the system address bus. The AEN is also used to disable other system bus drivers during DMA transfer.
10	HRQ	OUT	The 8237A uses this hold request signal to request the CPU for the system bus access authority.
11	$\overline{CS}$	IN	Chip selecting input.
12	CLK	IN	Clock input.
13	RESET	IN	Asynchronous, active high input used to clear the command, status, request, and temporary registers.
14 15 24 25	DACK 2 DACK 3 DACK 1 DACK 0	OUT	Indicates a DMA acknowledge to the peripheral logics.
16 17 18 19	DREQ 3 DREQ 2 DREQ 1 DREQ 0	IN	Independent, asynchronous channel request inputs used for peripheral logics to obtain DMA. DREQ 0 has the highest priority and DREQ 3 the lowest.
20	GND		0V pin.
21~23 26~30	DB7~DB0	OUT	Data bus output. During DMA cycle, high-order 8 address bits are output onto the data bus, and are loaded into an external latch by the ADSTB signal.
31	VCC	IN	+5V supply.
32~35	A0~A3	I/O	Low order 4 bits of the address bus. During idle cyles, these are input lines used for the 8237A to address the control register to be read or loaded. During active cycles, these are output lines used to furnish the low order 4 bits of address information.
36	$\overline{EOP}$	I/O	Information pertaining to the end of DMA is available at this pin. Low output = DMA end, or if forced LOW, forces DMA to end.
37~40	A4~A7	OUT	High order 4 bits of address bus. These lines are enabled only during DMA.

8. MFD INTERFACE CIRCUIT

8-1 Block diagram



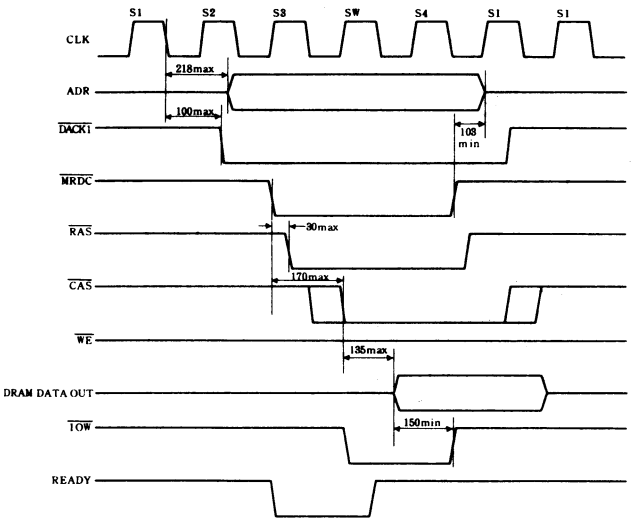
8-2 Operational description

For read or write to the FDD, data are transferred under the high speed mode using the 8237DMAC.
The following become necessary for the FDC to write or read the FDD.

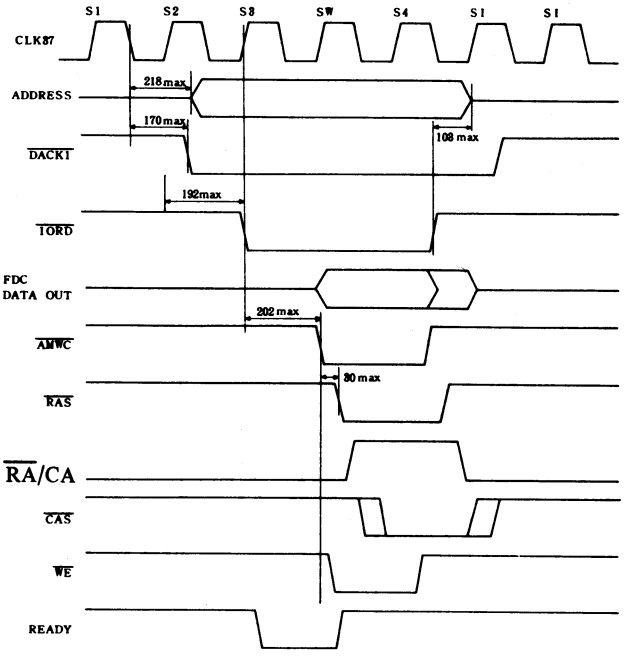
(1) The CPU furnishes the FDC and DMAC with command and parameter and the DMA channel 1 is opened.
(2) When the FDC finds the corresponding sector on the FDD, a DMA request (DRQ) is issued to the DMAC.
(3) When the DMAC receives DRQ, the DMAC issues a HRQ to the CPU.
(4) As the bus line is opened and HLDA signal is returned when the CPU receives HRQ, the DMAC sends back DACK signal to the FDC.
(5) Data transfer takes place between the FDC and the FDD under the bus control by the DMAC.

8-3 Timings

Memory to FDC

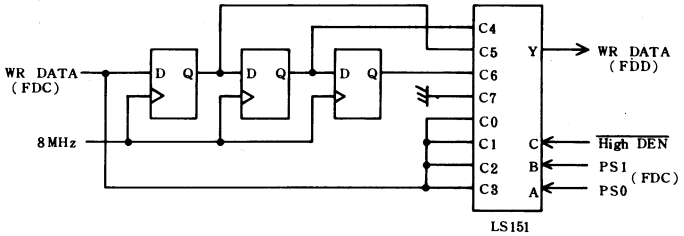


FDC to memory



8-4 Precompensation circuit

1. Block diagram

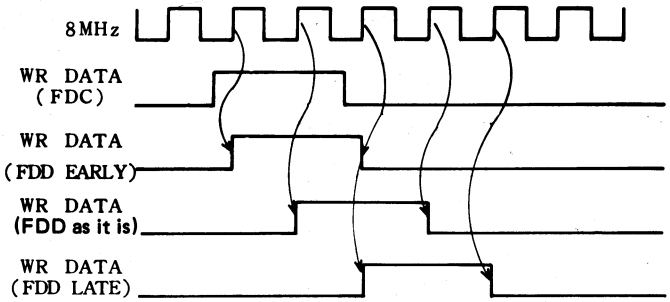


2. Operational description

The precompensation circuit is used to produce reading allowance by making compensation when writing the peak shift in the 640 KB MFM mode. As the FDC sends on PS0 and PS1 the compensation ratio at the time of write and the location of the write data is shifted according to the signal. However, precompensation is not done under the 640 KB FM mode and 1 MB mode.

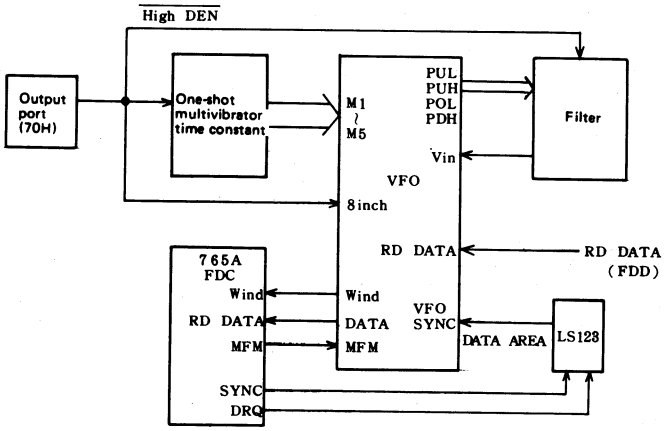
PS0	PS1	Precompensation shift —	WRDATA output
0	0	As it is	C4
0	1	LATE	C6
1	0	EARLY	C5
1	1	—	—

3. Timings



8-5 VFO circuit

1. Block diagram



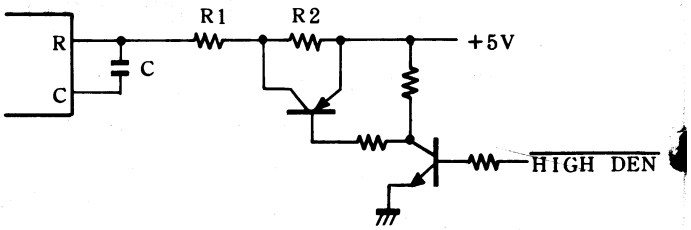
2. Operational description

The VFO circuit is used to distinguish the data section from the clock section when reading data from the FDD and is used to increase the reading margin to permit the window to follow a read data phase change fror such as a disk motor rotation change.

Four one-shot multivibrators of M1, M2, M4, and M5 are in the VFO.

M1: For read data phase comparison
M2: For SYNC byte detection
M4: For ID field separation
M5: For read data output pulse determination

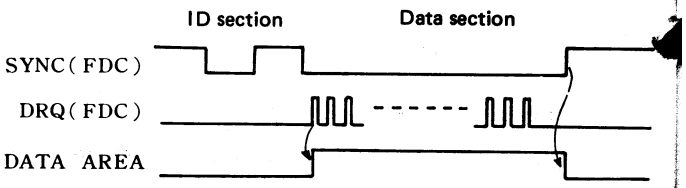
As M1, M2, and M4 need different time constant under the 1 MB mode and the 640 KB mode, it sould be attained in the following manner



When High Den = "0", the time constant must be CR1.
When High Den = "1", the time constant must be C(R1 + R2).

Also, M1 and M2 need to adjust as their pulse widths affect the reading margin.

When a SYNC byte is detected or when the ID field is recognized, the data are read exactly with an increased gain, and the gain is decreased in reading the actual data in order to achieve positive reading. For this purpose, DATA AREA signal is created from the FDC issued SYNC and DRQ to use it for switching of the gain level.



The signal after phase comparison pumps up and down the filter circuit, control the VCO oscillation frequency inside the VFO, and absorbs a change in the read data. (PLU, PDL ...Low gain, PUH, PDH...High Gain)

This filter circuit has also to be changed of the time constant under the 1 MB mode and the 640 KB mode.

3. VFO circuit adjustment

VFO circuit adjustment Potentiometers VR0 through 4 and the trimmer capacitor C60 are provided in the VFO circuit, which need to be adjusted again whenever the LSI or its components are replaced.

1) Special tools required
   Special VFO adjusting tool (UKOG-1011ACZZ)
   Oscilloscope of more then 100 MHz, having 50 ms, 0.1 μs, 0.1 μs, 0.2 μs, 0.5 μs, and 1 μs ranges.
2) Connection of the tool
   See the figure below for conection of the special tools.

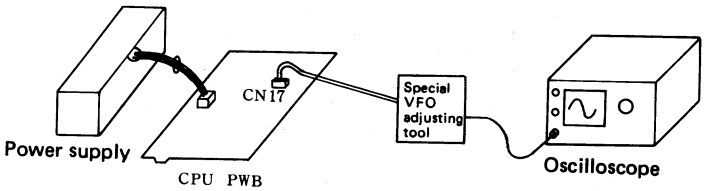


Fig. 1 Connection of special tools

3) Adjusting procedure
   a) Strap setup
      Observe the table below for connection of three straps provided on the PWB.

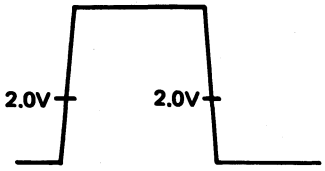
b) Adjustment

(1) Adjust the GND level of the oscilloscope.

(2) Set the switch to all OFF, connect the oscilloscope to point A and manipulate the potentiometer on the special tool to adjust it to 2.4 V. The oscilloscope voltage range at this point should be set to 1 V/scale notch with the frequency range at any point.

(3) Connect the oscilloscope to point B and change the oscilloscope frequency range to 0.05 microsecond. Next, manipulate the trimmer capacitor on the PWB to make the oscillation frequency synchronized to 247 ~ 252 nanoseconds.

(4) Set the switch to "1", connect the oscilloscope to point C and the oscilloscope frequency range to 0.1 microsecond and make it triggered at the rising edge of the signal. Manipulate the VR1 on the PWB to adjust the 2-V waveform to 2-V waveform to 2-V waveform distance to 495 ~ 505 nanosecond.



(5) Set the switch to "2" and the frequency range to 0.2 microsecond and manipulate the VR2 to set the 2-V waveform to 2-V waveform distance to 990 ~ 1010 nanosecond.

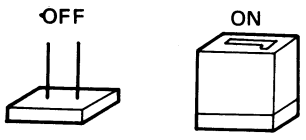
(6) Set the switch to "3" and the frequency rance to 0.5 microsecond and manipulate the VR3 to set the 2-V waveform to 2-V waveform distance to 2.48 ~ 2.52 microseconds.

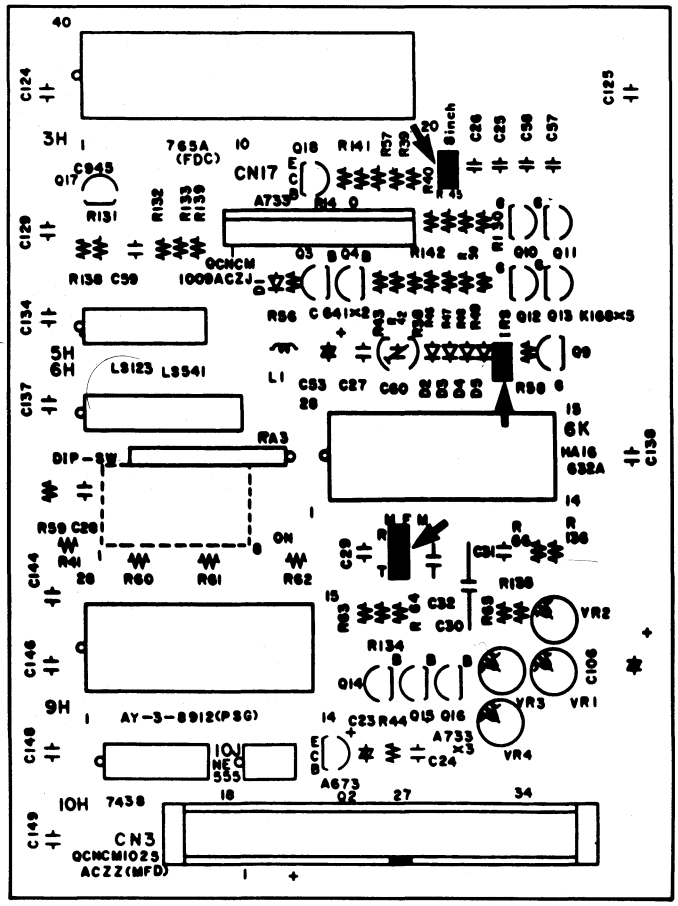
(7) Set the switch to "4" and the frequency range to 1 microsecond and manipulate the VR6 to set the 2-V waveform to 2-V waveform distance to 4.95 ~ 5.05 microseconds.

With the above procedure, the VFO adjustment is complate. Set straps as shown in Table 1-B and make potentiometers locked with paint.

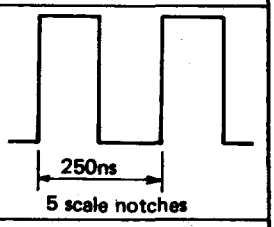
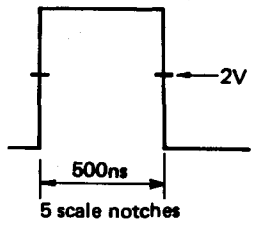
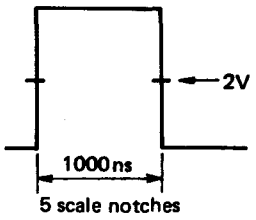
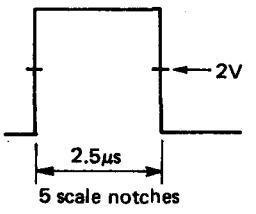
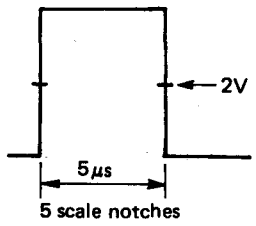
(See the succeeding table for strap locations)

Strap	8 inch	IRS	MFM
During VFO adjustment	OFF	ON	T side . . . ON R side . . . OFF
During operation	ON	OFF	T side . . . OFF R side . . . ON





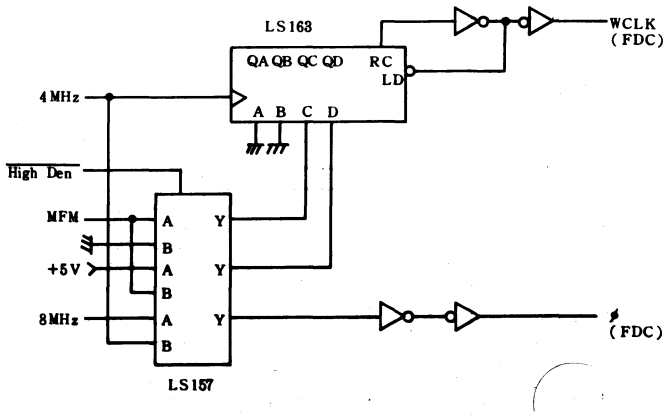
Procedure

No.	Test point on checker	Switch setting	Adjust point	Range	Oscilloscope	Waveform
1	A	–	Oscilloscope 0V level	–	0V	
2	B	All off	VR0 (on the tool)	–	2.4V (2.38 ~ 2.42V)	
3	C	All off	Trimmer capacitor on the C60 (PWB) VFO	0.05μs	4MHz (250ns) (247.5 ~ 252.5ns)	
4	C	SW1 → ON	VR1 (PWB)	0.1μs	500ns [High to high width] (495 ~ 505ns)	
5	C	SW2 → ON	VR2 (PWB)	0.2μs	1000ns [High to high width] (990 ~ 1010ns)	
6	C	SW3 → ON	VR3 (PWB)	0.5μs	2.5μs [High to high width] (2.48 ~ 2.52μs)	
7	C	SW4 → ON	VR4 (PWB)	1μs	5.0μs [High to high width] (4.95 ~ 5.05μs)	

NOTE: As the figures in the bottom are the range of values for adjustment, it is preferable to use the mean value.

8-6 FDC clock, write clock circuit

1. Block diagram



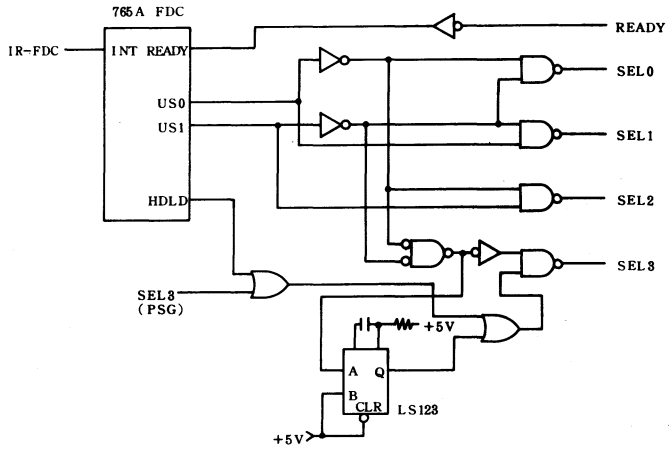
2. Operational description

Because the MFD interface circuit is used under the 1 MB mode and the 640 KB mode with the MZ-5600, it also needs to change the FDC clock and write clock, and in addition to it, the write clock has to be changed into the MFM and FM mode.

High Den	MFM	LS163C	LS163D	LS163 drive ratio	WCLK high width	FDCϕ
0	0	0	1	1/8	250ns	8MHz
0	1	1	1	1/4	↑	8MHz
1	0	0	0	1/16	↑	4MHz
1	1	0	1	1/8	↑	4MHz

8-7 MFD drive select circuit

1. Block diagram



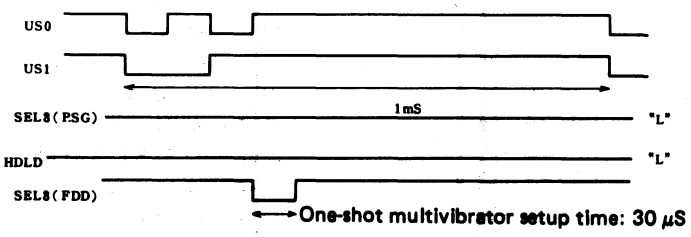
2. Operational description

The FDC searches each drive at 1 millisecond to check the ready state when not busy, that it, when waiting for a command. If the ready state searched before does not coincide with the ready state searched this time, it applied a state transition interrupt to the CPU to inform removal of the disk from the FDD.

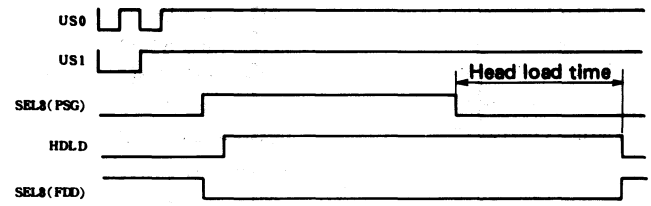
The reason why the one-shot multivibrator circuit is seen in the select of the drive 3 is to prevent the drive 3 front bezel lamp as if activating even when not being accessed. So, it needs to take OR with the select signal from the I/O port so far as the drive 3 is concerned.

3. Timings

- During search



- During access



8-8 FDC LSI (μPD765)

μPD765 Pin configuration (top view)

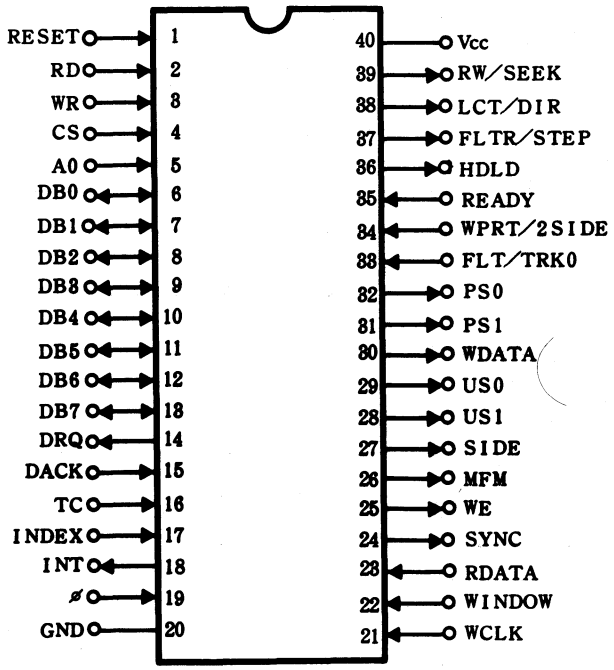


Fig. 45

μPD765 Block diagram

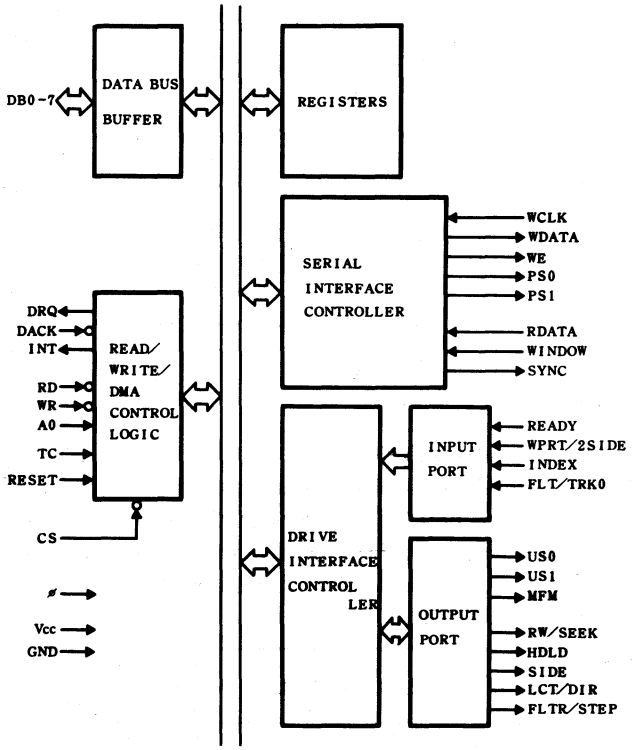


Fig. 46

RESET : Reset
RD : Read
WR : Write
CS : Chip Select
A0 : A0
DB0・7 : Data Bus
DRQ : DMA Regurst
DACK : DMA Acknowledge
TC : Terminal Count
INDEX : Index
INT : Interrupt Reguest
ø : Clock
GND : Ground
WCLK : Write Clock
WINDOW : Data Window
RDATA : Read Data
SYNC : VFO Synchronize
WE : Write Enable

MFM : MFM Mode
SIDE : Side Select
US0, 1 : Unit Select
WDATA : Write Data
PS0, 1 : Pre Shift
FLT : Fault
TRK0 : Track 0
WPRT : Write Protected
2SIDE : Two Side
READY : Ready
HDLD : Head Load
FLTR : Fault Reset
STEP : Step
LCT : Low Current
DIR : Direction
RW/SEEK : Read Write/Seek

μPD765 Pin functions Table 22

Pin No.	Function	I/O	Description
40	VCC	–	+5V
20	GND	–	0V
19	φ	I	Single-phase clock (TTL compatible)
1	RESET	I	Places the FDC in the idle state and sets all the drive interface outputs to low, with the exception of PS0, PS1, and WDATA (indefinite) outputs. Also sets the INF and DRQ outputs to low. The DB is placed int he input state.
4	CS	I	Makes the RD and WR signals valid.
13~6	DB7~DB0	I/O	Bidirectional, three-state data bus.
3	WR	I	Control signal sued to write data into the FDC via the data bus.
2	RD	I	Control signal used to read data out of the FDC via the data bus.
18	INT	O	Indicates the FDC is requesting service. During non-DMA mode, this is output for each transfer byte; during DMA mode, this is output at the end of command execution.
5	A0	I	Selects the status and data registers within the FDC which are to be accessed through the data bus. If A0 is zero, the status register is selected; if it is one, the data register is selected.
14	DRQ	O	DMA request used to request DMA transfer between the FDC and memory.
15	DACK	I	Indicates a DMA request has been acknowledged. During DMA cycles, this signal functions in the same way as the CS.
29, 28	US0, 1	O	Drive select lines. Up to four FDD's can be selected by decoding these two lines.
26	MFM	O	Specifies the VFO logic operation mode. If MFM is one, specifies the MFM mode; if MFM is zero, specifies the FM mode.
24	SYNC	O	Specifies the VFO logic operation mode. If SYNC is one, read operation is enabled; if it is zero, read operation is disabled.
39	RW/SEEK	O	Distinguishes between the signal which functions as both read/write and seek signals, from the drive interface signals. If RW/SEEK is zero, indicates R/W; if it is one, indicates SEEK.
36	HDLD	O	Loads the read/write head in the drive.
27	SIDE	O	Selects head 0 or 1 of a double-sided drive. If SIDE is zero, head 0 is selected; if it is one, head 1 is selected.
38	LCT/DIR	O	If the R/W SEEK signal specifies R/W, this signal functions as the LCT to indicate the drive's read/write head is accessing cylinder 43 or above. If the R/W SEEK signal specifies SEEK, this signal functions as the DIR, which specifies the direction of the seek operation. If DIR is zero, a seek operation is done toward the edge of the disk; if it is one, the seek operation is done toward the center of the disk.
37	FLTR/STEP	O	If the R/W SEEK signal specifies R/W, this signal functions as the FLTR and is used to reset the fault condition which is retained on the drive. If it specifies SEEK, this signal functions as the STEP and becomes the step signal for seek.
35	READY	I	Indicates the drive is in the ready state.
34	WPRT/2 SIDE	I	If the R/W SEEK signal specifies RW, this signal functions as the WPRT to indicate the drive or medium is write protected. If it specifies SEEK, this signal becomes 2 SIDE to indicate a double-sided medium is placed in the drive.
17	INDEX	I	Indicates the physical beginning of the tracks on the medium.
33	FLT/TRK0	I	If the R/W SEEK signal specifies RW, this signal functions as the FLT to indicate the drive is in the fault state. If it specifies SEEK, this signal functions as the TRK0 to indicate the read/write head is positioned on cylinder 0.
16	TC	I	Indicates the completion of a read or write operation from the host system.
30	WDATA	O	Write data to the drive, comprised of clock and data bits.
25	WE	O	Specifies a write operation to the drive.

<table>
<tr><th>Pin No.</th><th>Function</th><th>I/O</th><th>Description</th></tr>
<tr><td>21</td><td>WCLK</td><td>I</td><td>Write data timing signal to the drive. 250kHz when in the FM mode, and 500kHz when in the MFM mode.</td></tr>
<tr><td>32, 31</td><td>PS0, 1</td><td>O</td><td>Used to specify whether writing data is to be delayed or advanced by a specified interval during a write operation in the MFM mode, to ensure a read margin. These signals control the WDATA signal as follows:
<table>
<tr><th>PS0</th><th>PS1</th><th>FM</th><th>MFM</th></tr>
<tr><td>0</td><td>0</td><td>No time change</td><td>No time change</td></tr>
<tr><td>0</td><td>1</td><td>–</td><td>LATE
225 ~ 250 ns</td></tr>
<tr><td>1</td><td>0</td><td>–</td><td>EARLY
225 ~ 250 ns</td></tr>
<tr><td>1</td><td>1</td><td>–</td><td>–</td></tr>
</table></td></tr>
<tr><td>23</td><td>RDATA</td><td>I</td><td>Data read from the drive, comprising clock and data bits.</td></tr>
<tr><td>22</td><td>WINDOW</td><td>I</td><td>This is created in the VFO logic to sample the RDATA.
Phase synchronization between RDATA bits and the WINDOW signal is done within the FDC.</td></tr>
</table>

(1) Medium sensor

The host system identifies whether or not a diskette is placed in the drive, by first sending a SENSE DEVICE STATUS command to the FDC, then reading the result status (ST3) from the FDC, and identifying whether the MFD is in the READY state or not.

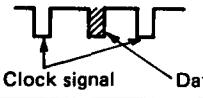
If the MFD remains NOT READY 800ms after its motor is turned on, the host identifies that no disk is in that MFD.

8-9 VFO LSI (HA16632P)

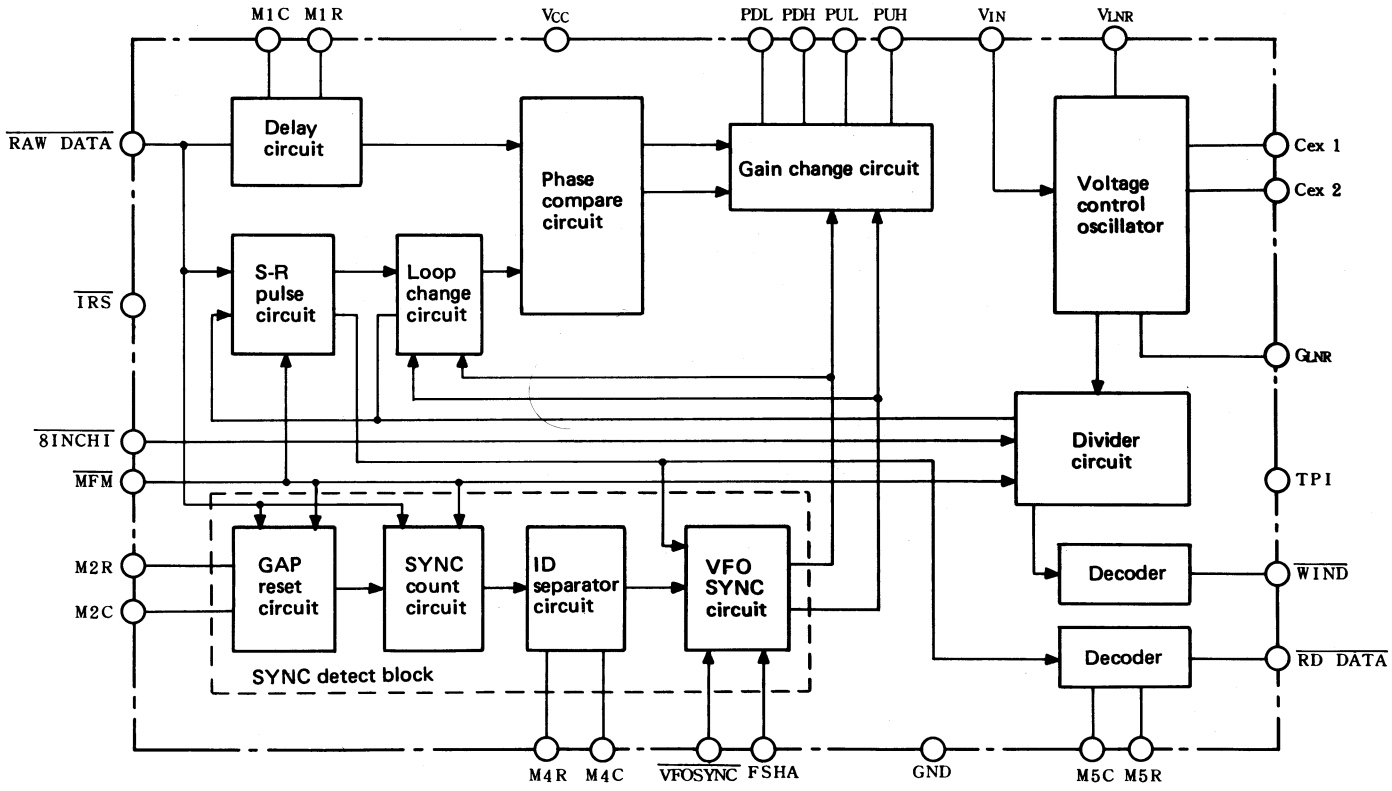
8-9-1. Characteristics

- By a high/low change of the control pin, it makes connection possible to the 8" or 5" floppy disk drive.
- By a high/low change of the control pin, it makes input possible to the double-density or single-density media.
- By a high/low change of the control pin, it makes connection possible to any of the UPD765, MB8866, or FD1791 floppy disk controller.
- The input/output circuit consists of the LS-TTL circuit.

8-9-2. Signal description

Pin No.	Signal name	In/Out	Description	Note
1	WIND	Out	1. Clock contained in RAW DATA signal and the window signal output line used to distinguish the data signal (when *$\overline{IRS}$=high). 2. One-shot multivibrator M1 output monitor line (when *$\overline{IRS}$=low).	
2	$\overline{DATA}$	Out	1. Waveform shaped read data output (when *IRS=high). 2. One-shot multivibrator M2 output monitor line (when *IRS=low).	
3 4	M5C M5R	In In	One-shot multivibrator M5 capacitor connection pin One-shot multivibrator M5 resistor and capacitor connection pin	
5	$\overline{VFO\ SYNC}$	In	Input to indicate detection of SYNC byte. When FSHA is low, gain is changed with this signal for loopback. SYNC byte detected when VFO SYNC is low. SYNC byte not detected when VFO SYNC is high.	
6	$\overline{FSHA}$	In	Input to assign the floppy disk controller type. $\overline{FSHA}$=Low → MB8876, 8877 $\overline{FSHA}$=High → μPD765	As the external SYNC field correction circuit is provided with the MZ-5600, it is used with a high state of *$\overline{FSHA}$.
7 8	M4R M4C	In In	One-shot multivibrator M4 resistor and capacitor connection pin One-shot multivibrator M4 capacitor connection pin	
9	GND	In	GND (0V) for all blocks except for the VCO block	
10 11	M2R M2C	In In	One-shot multivibrator M2 resistor and capacitor connection pin One-shot multivibrator M2 capacitor connection pin	
12	MFM	In	Input line to assign two choices of the FM and MFM modes (high for the FM mode and low for the MFM mode)	
13	RD DATA	In	Raw data from the floppy disk Includes two signal components of (1) clock signal and (2) data signal.	
14	TP1	In	IC test pin When *IRS is high, loop change circuit output is monitored. When *IRS is low, VFO SYNC circuit output is monitored.	
15 16 17	V_{CC} M1R M1C	In In In	5V supply for all circuit except the VCO block One-shot multivibrator M1 resistor and capacitor connection pin One-shot multivibrator M1 capacitor connection pin	
18	$\overline{IRS}$	In	IC test pin *$\overline{IRS}$ high when in connection *$\overline{IRS}$ low during the IC test	
19 20	$\overline{PDL}$ $\overline{PDH}$	Out Out	Charge pump down output for low gain (DATA loop) Charage down output for high gain (SYNC loop)	
21 22	PUL PUH	Out Out	Charge pump down output for low gain (DATA loop) Charage down output for high gain (SYNC loop)	
23	GLNR	In	VCO block GND	
24 25	CEX1 CEX2	In In	VCO capacitor connection pin VCO capacitor connection pin	
26	VIN	In	VCO oscillation frequency control voltage input	
27	VLNR	In	VCO block supply voltage (5V)	
28	$\overline{8\ INCH}$	In	1. Input to indicate the data read source; 8" FDD or 5" FDD (IRS=high). $\overline{8\ INCH}$=Low → 8 INCH FDD $\overline{8\ INCH}$=High → 5 INCH FDD	

8-9-3. Internal block diagram



9. PRINTER INTERFACE

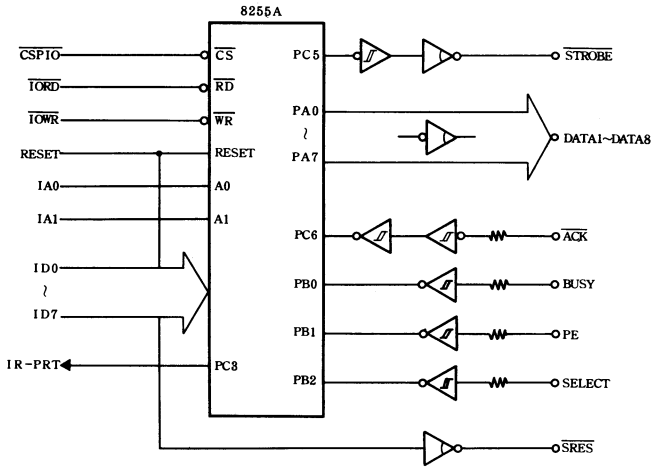


Fig. 48

9-1 Logic description

The printer interface uses an integral parallel interface controller, 8255. The 8255 has the modes shown in the table at the right. Group A of the 8255 is used in Mode 1 for Centronics interface, so that the CPU may be interrupted by an $\overline{ACK}$ signal from the printer by Mode 1 function.

Table 24

Mode 1 output	PA 0 ~ PA7	
	PC7	
	PC6	$\overline{ACK}$
	PC5	OUT
	PC4	OUT
	PC3	INT
Mode 0 output	PC2	
	PC1	OUT
	PC0	
Mode 0 input	PB0 ~ PB7	IN

9-2 Control procedure

(1) Check if the printer is busy.
(2) Output printed data to port A of 8255.
(3) Reset the PC5 bit ($\overline{\text{STROBE}}$).
(4) Set the PC5 bit ($\overline{\text{STROBE}}$).
(5) Set the PC6 bit (INTE flag) to enable interrupts.
(6) Wait for an interrupt (INT).
(7) Reset the PC3 bit (INT) of the 8255.
(8) Output the next printed data to port A.
(9) Reset the PC5 bit ($\overline{\text{STROBE}}$).
(10) Set the PC5 bit ($\overline{\text{STROBE}}$).
(11) If the printed data is the last piece of data, reset the PC6 bit (INTE) to disable the interrupt.
(12) If it is not the last piece of data, wait for an interrupt.

9-3 Parallel interface signals

Table 25

Pin No.	Signal name	Direction	Description
1	$\overline{\text{STROBE}}$	→ PRINTER	Printer samples print data at the leading edge of this signal.
2	DATA1	→ PRINTER	Print data
3	DATA2		
4	DATA3		
5	DATA4		
6	DATA5		
7	DATA6		
8	DATA7		
9	DATA8		
10	$\overline{\text{ACK}}$	← PRINTER	Character input complete or function complete.
11	BUSY	← PRINTER	Data receive ready: Low
12	PE	← PRINTER	Paper end: High
24	$\overline{\text{SRES}}$	→ PRINTER	Reset signal
25	SELECT	← PRINTER	Indicates the selected state (receive ready): High

* 14~23 GND
* 13

9-4 Timing chart

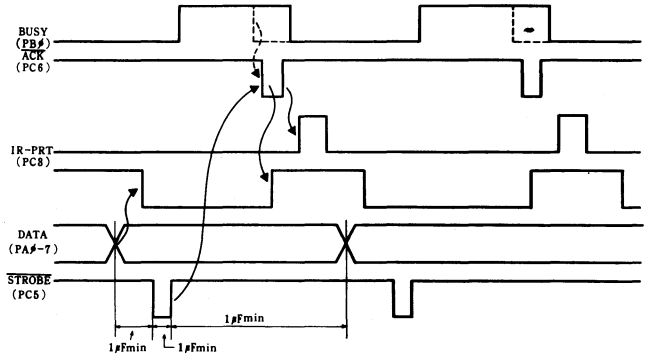
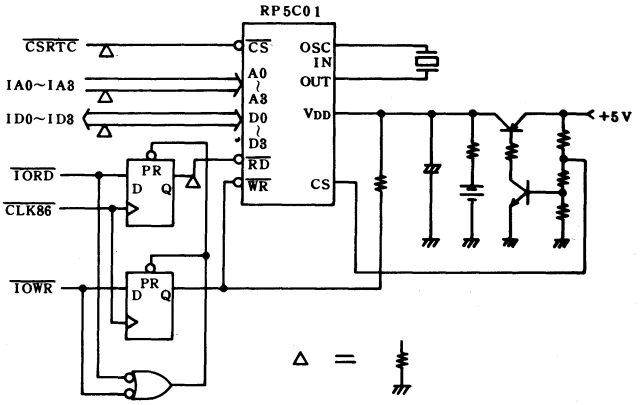


Fig. 49

10. RTC REAL TIME CLOCK

10-1 Block diagram



10-2 Operational description

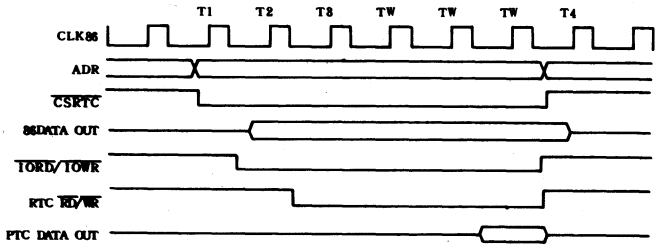
The RP5C01 is used for the real time clock of the MZ-5600 and is connect parallel to the 8-bit I/O bus. Each of the second, minute, hour, day of week, day, month, and year registrers are allocated to thirteen addresses and represented in a BCD number.

As there is an alarm register apart from the calendar registers, it is possible to interrupt the CPU when the time set in the alarm register just meet the time in the calendar resiters. They incorporate two 13 x 4 battery backed up RAMs.

In order to set voltage stable for input and output pins during power off, the real time clock is resistor pulled down, except for *WR signal which is pulled up to prevent error writing of data at the time of power on and off.

*RD and *WR are delayed by the flipflop in order to maintain the address setup time for command.

10-3 Timing-chart

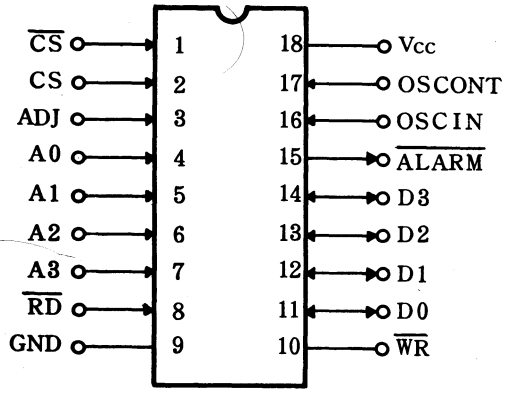


10-4 RP5C01 (real-time clock)

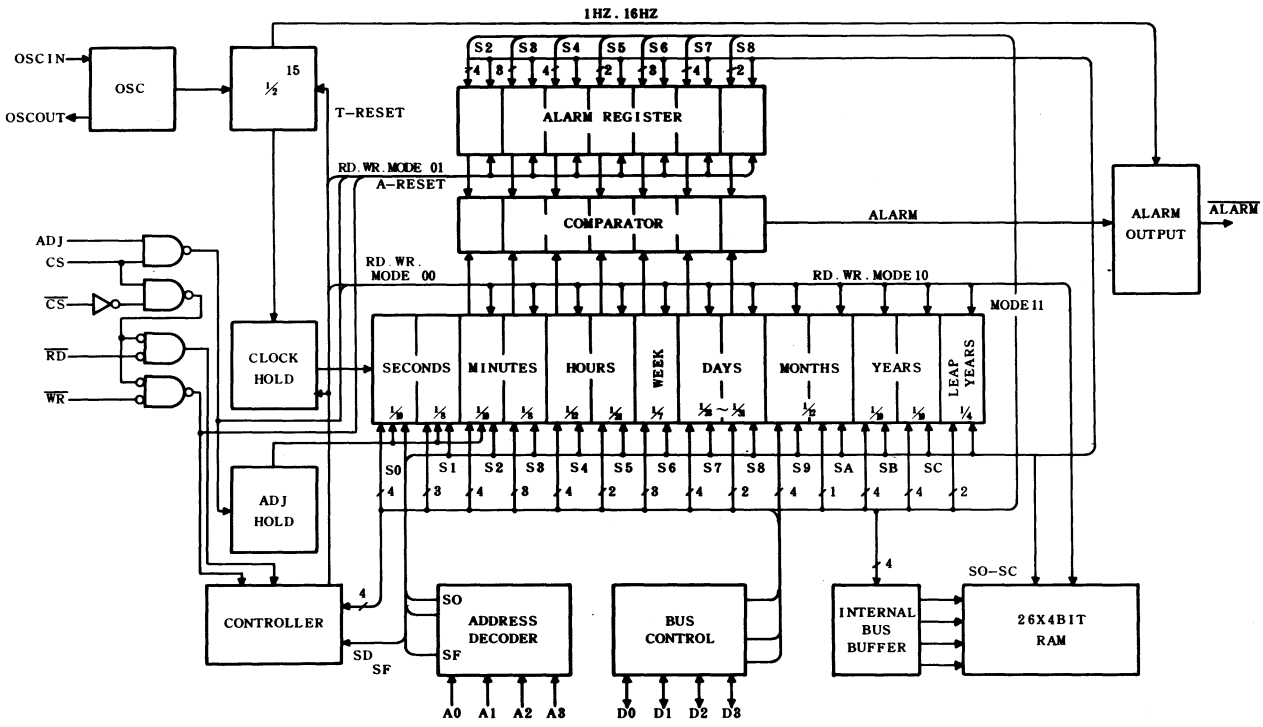
(1) Highlights

1) Able to be connected directly to the CPU.
2) Available as either a 24 hours or 12 hours, AM/PM clock.
3) Contains a leap year calendar.
4) All time data is output in BCD codes.
5) Adjustable by trimmer capacitor
6) Allows a battery back-up.
7) Built-in 26 x 4 bit RAM.
8) A timing pulse of 1Hz or 16Hz available as an alarm.

(2) Pin configuration



(3) Block diagram



(4) Pin functions Table 26

Pin No.	Signal name	I/O	Description
1	CS	IN	Chip selector
2	CS	IN	Power down sense input
3	ADJ	IN	Used to adjust the seconds of the real clock without using the CPU.
4~7	A0~A3	IN	Address bus
8	RD	IN	Read control output
9	GND	IN	0V pin
10	WD	OUT	Write control output
11~14	D1~D3	I/O	Data bus
15	ALARM	OUT	Provides a 1Hz or 16Hz pulse as an alrm
16~17	OSC I/O	I/O	Accepts a quarts-oscillator
18	Vcc	IN	+5V power supply

11. PROGRAMMABLE SOUND GENERATOR INTERFACE

11-1 Block diagram

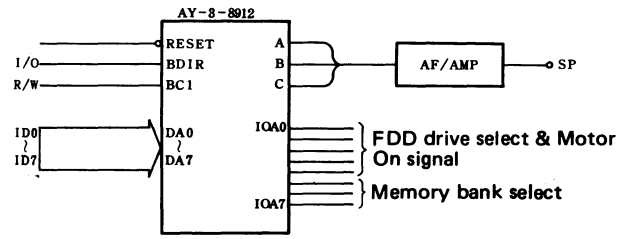


Fig. 54

11-2 Logic description

The programmable sound generator, AY-3-8912 has three independent sound outputs to produce chords.
It contains a general-purpose 8-bit I/O port, and uses the IOA0—IOA4 as the FDD drive selector and motor on signals, and the IOA5—IOA7 as a bank selector for the memory area A0000H through BFFFFH.

11-3 Programmable sound generator (PSG) AY-3-8912

(1) Highlights

1) Completely software-controlled sound generation.
2) Interfaces with almost all 8 or 16-bit microprocessors now available.
3) Three independent programmable analog outputs.
4) 8-bit general-purpose I/O port.
5) Single +5V power supply.

(2) Pin configuration

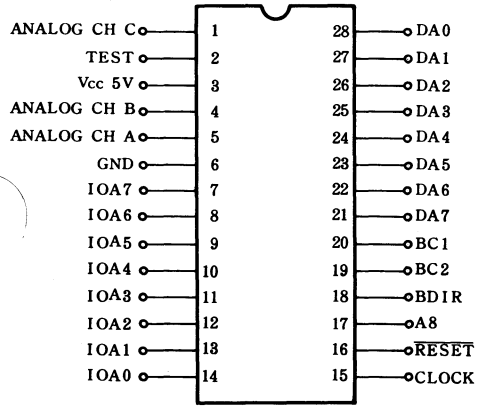
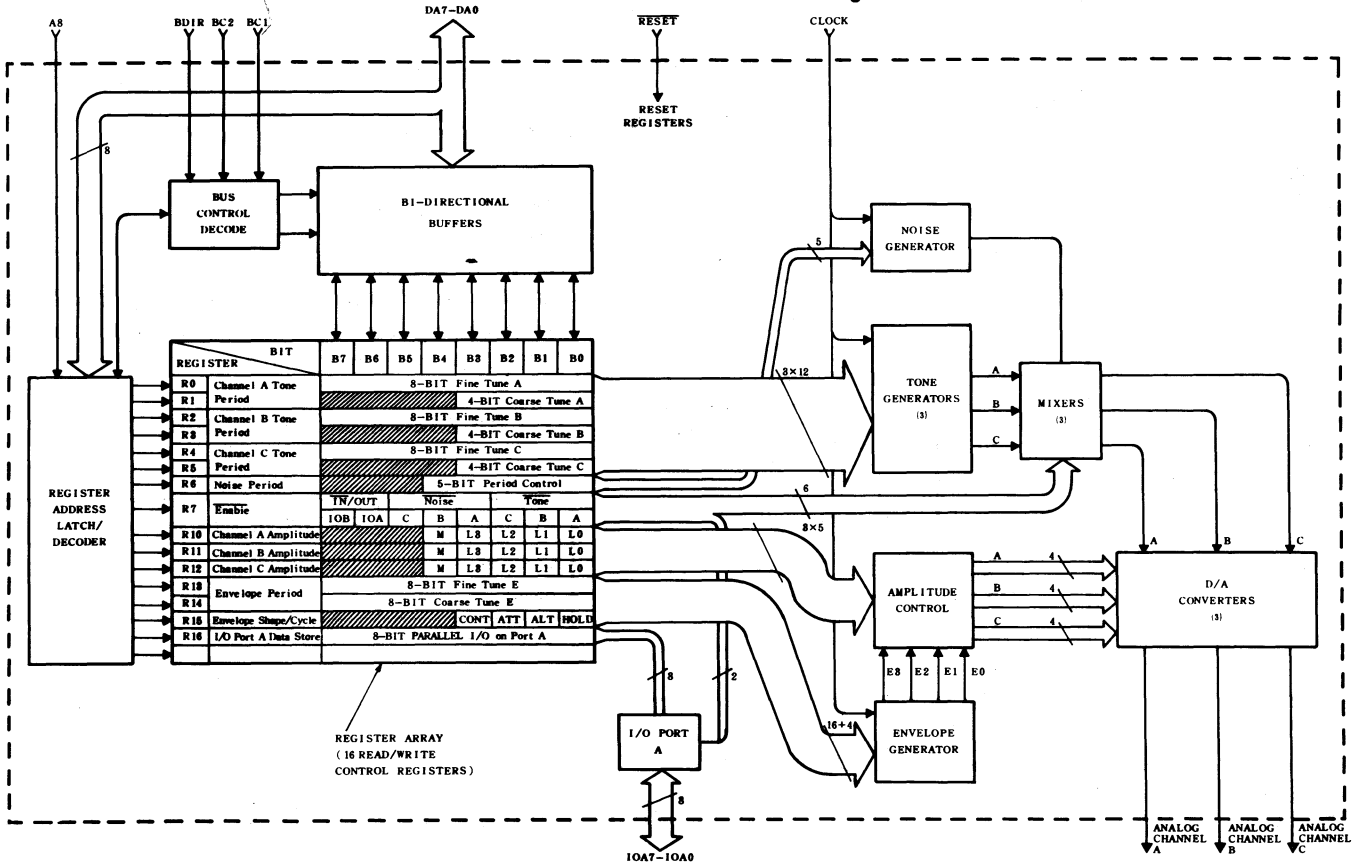


Fig. 55

(3) Block diagram



(4) Pin functions

Table 27

Pin No.	Signal name	I/O	Description
1	ANALOG CH C	OUT	Analog output channel C
2	TEST1		Line test pin (must be unconnected).
3	Vcc		+5V power supply.
4	ANALOG CH B	OUT	Analog output channel B
5	ANALOG CH A	OUT	Analog output channel A
6	GND		0V pin
7~14	IOA7~0	I/O	I/O port
15	CLOCK	IN	Reference timing input for tone noise and envelope generators.
16	$\overline{\text{RESET}}$	IN	All internal registers are reset by applying a low level to this input at the time of power up.
17	A8	IN	Auxiliary address bit used to allocate not only the areas specified by DA0~DA7, but also extended memory space.
18	BDIR	IN	Bus direction — These bus control signals control all the buses, internal or external, in the PSG. The PSG decodes these signals as follows:
19	BC2	IN	Bus control 2
20	BC1	IN	Bus control 2

BDIR	BC2	BC1	PSC function	
0	0	0	INACTIVE:	PSG/CPU bus is inactive, and DA0~DA7 are set to a high impedance.
0	0	1	ADDRESS LATCH:	Indicates the register address to be latched into the PSG is on the bus.
0	1	0	INACTIVE:	
0	1	1	READ FROM PSG:	Transfers the contents of the currently addressed register to the PSG/CPU bus.
1	0	0	ADDRESS LATCH:	
1	0	1	INACTIVE:	
1	1	0	WRITE TO PSG:	Indicates the register data to be latched into the currently addressed register is on the bus.
1	1	1	ADDRESS LATCH:	

21~28	DA7~DA0	I/O	When in Data mode: Corresponds to the register array bits B0~B7. When in Address mode: DA0~DA3 selects a register number, and DA4~DA7 is used for address input.

12. RS-232C INTERFACE

12-1 Logic description

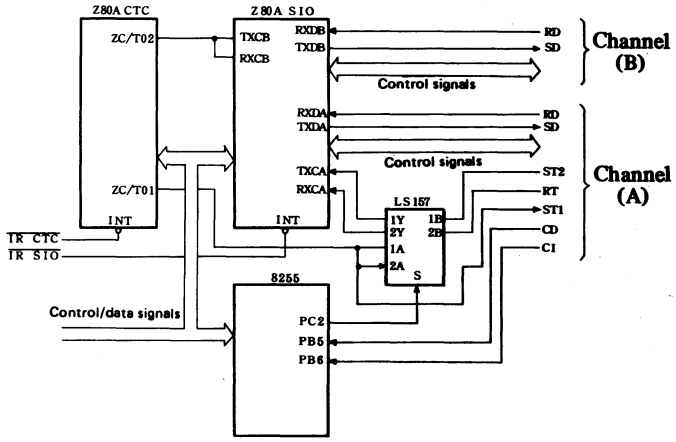


Fig. 57

The RS-232C serial data interface has two channels, one of which may be used for synchronous transmission. For internal synchronization, the Z80CTC supplies a baud rate clock for 100–9600 bauds to the SIO under software control.

To allow external synchronization for channel A, the LS157 is switched by the PC2 output of the 8255, so that the clock for the SIO may be furnished either from the Z80CTC or an external source.

12-2 RS-232C interface specifications

Table 28

I/O format	RS-232C bit serial input/output
Channel	Two channels
Code	ASCII 7/8 bit code
Baud rate:	110~9600 bps
Synchronization scheme:	CH. A (synchronous/start-stop or acynchronors). CH. B (asynchronous start-stop)
Data format	Stop bit: 1/1.5/2 Parity: Even/odd/none
LSI chip used:	Z80 SIO and Z80A CTC

Channel A is synchronous, and may be used for BSC protocol.

* Binary synchronous communication (BSC):
The BSC is a character-type communication protocol, in which a series of standard control characters are used for synchronous binary data transmission between offices for data communications.

12-3 Serial interface signal lines

Channel A: Usable for both asynchronous and synchronous (BSC) communications.

Note: When interfacing one device to another via the RS-232C interface, the transmission rate, word length, parity bit, and stop bit on each device must first be set up identically. The signal lines to be used will differ depending on individual devices. Therefore, the user must have a full understanding of the signal lines and their functions used for the interface.

Input/output signal pin functions

Table 29

Pin No.	Mnemonics	Signal name	Signal direction	Description
1	SG (FG)	Signal ground (Fram ground)		*1
2	SD	Send data	OUT	Data sent by the MZ-5500
3	RD	Receive data	IN	Data received by the MZ-5500
4	RS	Request to Send	OUT	In CP/M-86 or BDOS: Always off. In BASIC: On during data send Turned off at the end of data send.
5	CS	Clear to send	IN	Response to Request to Send: If this signal is on, the system sends data. If it is off, the system stops data send. Note: Up to two bytes of data may be sent after the CS is turned off.
6	READY (DTR)	Data Terminal Ready	OUT	Indicates whether or not the system is ready for data reception: READY is on if the system is ready. READY is off if the system is not ready.
7	SG	Signal Ground		*1
8	DR (DSR)	Data set Ready	IN	Indicates whether or not the remote device is ready for operation. On if the remote device is ready for data send/receive. Off if the remote device is not ready for data send/receive. If this signal is turned off during data send/receive operation, an error will result. *2
9	SG	Signal Ground	IN	*1
12	ER	Equipment Ready	OUT	Always on as long as the system power is on.
While the MZ-5600 system has the following additional signal lines, they are not supported in the CP/M-86FDOS or BASIC (only channel A).				
10	CD	Carrier Detect	IN	Indicates the remote device is a sending carrier.
11	CI	Call Indication	IN	Indicates a termination call has arrived from the line.
13	ST1	Transmitter signal element timing	OUT	Outputs a send signal element timing information for synchronous communications. (DTE source)
14	RT	Receiver signal element timing	IN	Inputs receiver signal element timing for synchronous communications. (DCE source)
15	ST2	Transmitter signal element timing	IN	Outputs (from device) send signal element timing for synchronous communications. (DCE source)

*1. Pins 1, 7, and 9 are signal grounds.
*2. The CS and DR pin functions may be disabled. For more details see the description of the RSPARM and IOCNF in the CP/M-86 User's Manual.
*3. For the details of the CD, CI, ST1, RT, and ST2, see the Owner's Manual.

MZ-5600 interconnection example

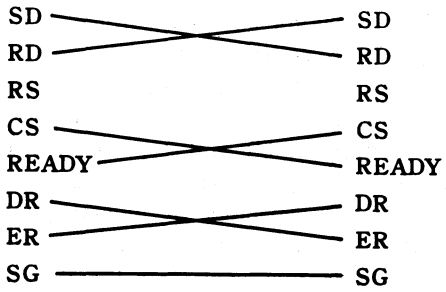


Fig. 58

Functional specifications
(Electrical characteristics)

Control signals: RS, CS, READY, DR, ER, CD, CI, ST1, ST2, and RT
On voltage: +5 to +15V
Off voltage: −5 to −15V

Data signals: SD and RD
Mark: −5 to −15V
Space: +5 to +15V

Baud rate: 110, 150, 200, 300, 600, 1200, 2400, 4800, or 9600 bauds

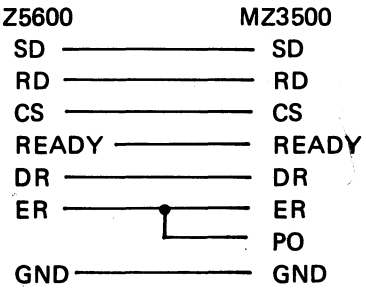
Word length: 7 or 8 bits

Parity: Even, odd, or none

Stop bit: One bit, one and Half, two bit

Protocol: Start-stop asynchronous non-protocol

- MZ5600 between MZ3500 connection



Others are OPEN

Dip SW	
5	ON
6	ON
7	OFF

- Software EXP.) BASIC 3

[MZ6500, MZ5500] → [MZ3500]

```
10  CHANNEL 1, 9600, "8N2"
20  SEND "MZ-5500"; "@";
30  END
```
MZ5600

```
10  CHANNEL 0, 9600, "8N2"
20  RCV A$, 0, "@"
30  A$ = LEFT$ (A$, LEN A$-1)
40  DISP A$ = END
```
MZ3500

[MZ3500] → [MZ5500]

```
10  CHANNEL 0, 9600, "8N2"
20  SEND "MZ-3500"; "@";
30  END
```
MZ3500

```
10  CHANNEL 1, 9600, "8N2"
20  RCV A$, 0, "@"
30  A$ = LEFT$ (A$, LEN A$-1)
40  DISP A$ = END
```
MZ5600

12-4 Z80A SIO (LH0084A) Pin configuration

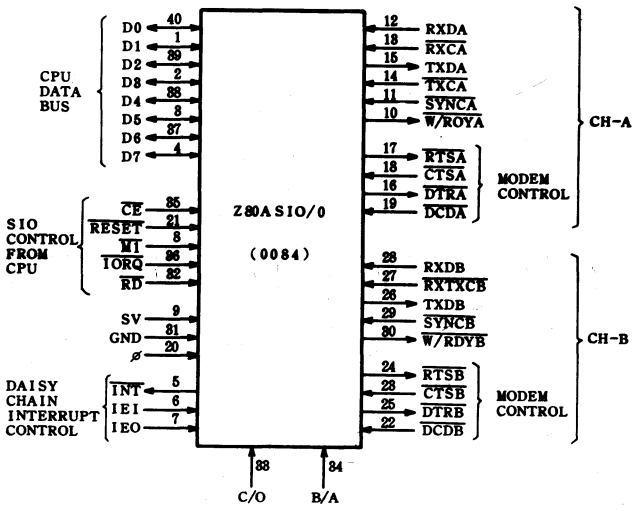


Fig. 59

D0-D7: System data bus used for data or command transfer between the CPU and Z80 SIO.

B/$\overline{A}$: Channel A or B select (high for B, low for A).

C/D: Control (command) or data select (high for control, low for data).

$\overline{CE}$: Chip enable

$\overline{M1}$: Machine cycle 1

$\overline{IORQ}$: I/O request

$\overline{RD}$: Read cycle status

$\overline{RESET}$: Reset

IEI: Interrupt enable input

IEO: Interrupt enable output

$\overline{INT}$: Interrupt request

$\overline{W/RDYA}$, $\overline{W/RDYB}$: Wait/Ready A, Wait/Ready B

$\overline{CTSA}$, $\overline{CTSB}$: Indicate send ready.

$\overline{DCDA}$, $\overline{DCDB}$: Data carrier detect; indicate send/receive ready.

$\overline{RXDA}$, $\overline{RXDB}$: Received data.

TXDA, TXDB: Send data

$\overline{RXCA}$, $\overline{RXCB}$: Receiver clock. In the synchronous mode, the RXC has the same rate (frequency) as the baud rate used. In the asynchronous mode, the RXC has a rate which is a multiple of the baud rate used: i.e. 1, 16, or 64 times the baud rate depending on the mode instruction.

$\overline{TXCA}$, $\overline{TXCB}$: Transmitter clock; functionaly the same as RXC, for transmission.

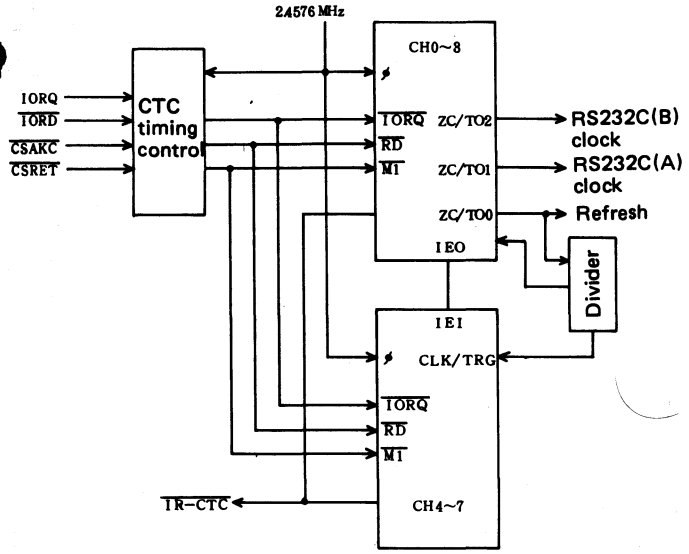
$\overline{RTSA}$, $\overline{RTSB}$: Request to Send to peripheral devices.

$\overline{DTRA}$, $\overline{DTRB}$: Data Terminal Ready sent to peripheral devices.

$\overline{SYNCA}$, $\overline{SYNCB}$: Synchronization signal input

13. SOFTWARE TIMER

13-1 Block diagram



13-2 Operational description

Two Z80A CTC are used for the software timer, and it has eight channels; each one having specification described in the next paragraph.

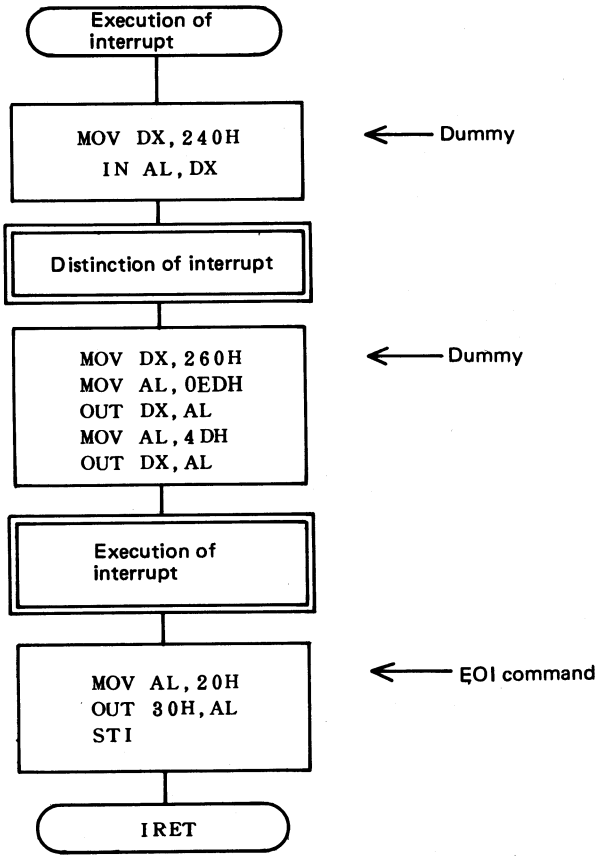
Timing control circuit is adopted in order that the 8086 CPU may control I/O read, write, interrupt acknowledge, and interrupt restore cycles of the Z80A CTC. As the 8086 CPU has no interrupt acknowledge and interrupt restore cycles, the following procedure is given using the I/O port (*CSAKC, *CSRET). For the interrupt acknowledge cycle, the interrupt vector outputted from the CTC is sent to the AL register when read through the I/O port (240H). For the interrupt restore cycle, the data equals to "RET1" of the Z80 CPU when writing "0EDH" or "04DH" to the I/O port (260H).

13-3 Channel description

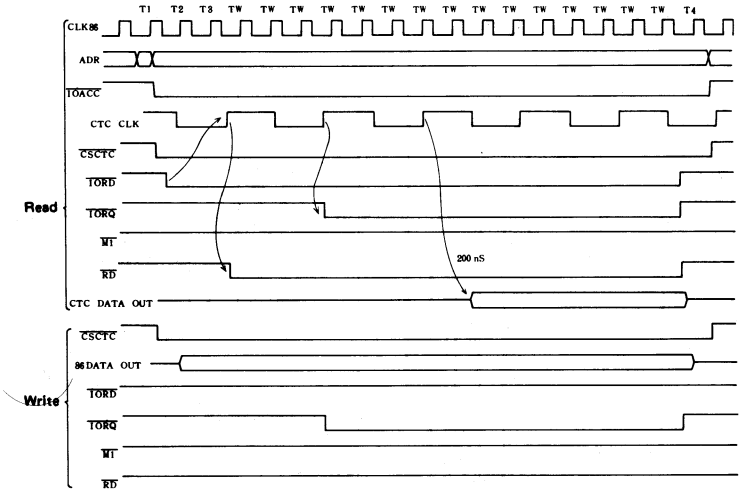
CH No.	I/O ADR	MODE	PRESCALE	INT	Time Constant etc	
0	210H	Timer	1/16	X	2	Refresh timer; 153/2 ms
1	211H	↑	↑	X	1 9600 b/s 2 4800 4 2400 8 1200	RS-232-C CHA Tx, Rx
2	212H	↑	↑	X	16 600 32 300 64 150 87 110	RS-232-C CHB Tx, Rx
3	213H	Counter		O	0.832 mS ~ 213 mS	System Timer
4	214H	↑		O	0.052 mS ~ 13,313 mS	Reserved
5	215H	↑		O	0.832 mS ~ 213 mS	For SEEG version only
6	216H	↑		O	0.832 mS ~ 213 mS	Reserved
7	217H	↑		O	3.328 mS ~ 852 mS	Reserved

13-4 Interrupt processing

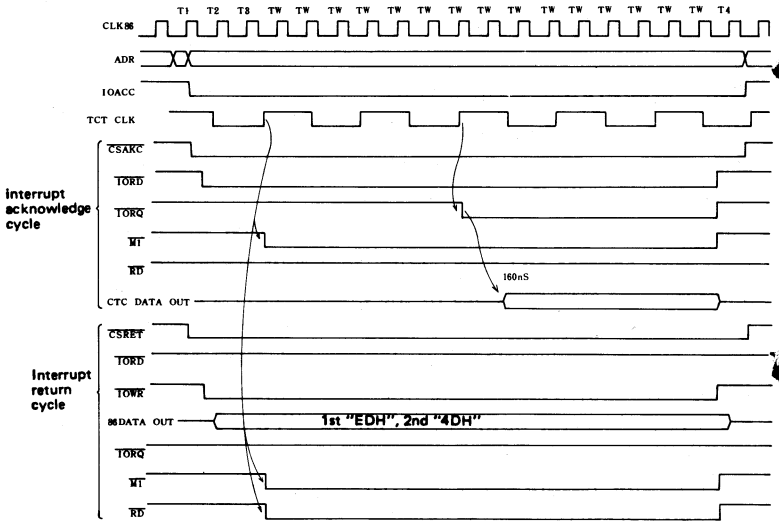
For the Z80A CPU, interrupt is processed by the hardware, and for the MZ-5600, it is processed by the software.
Because the interrupt controller 8259A control interrupt to the MZ-5600, it needs to issue the interrupt terminante command (EOI) to the 8259A in case it is possible to accept an interrupt of higher priority at the end of the interrupt processing routine.



13-6-1 Timing chart



13-6-2 Timing chart



13-5 Distinction of interrupt channel

The Z80A CTC issues the interrupt vector in the interrupt acknowledge cycle. As the vector contents are set in the AL register when the MZ-5600 executes the dummy interrput acknowledge cycle, the interrupt channel can be known from the contents.
However, as the vector "0H" has already been set to the CTC-1, the CTC-2 must have the vector of "08H" set.

Ch	VECTOR
3	06 H
4	08 H
5	0 AH
6	0 CH
7	0 EH

13-7 Z80A CTC

CTC pin configuration

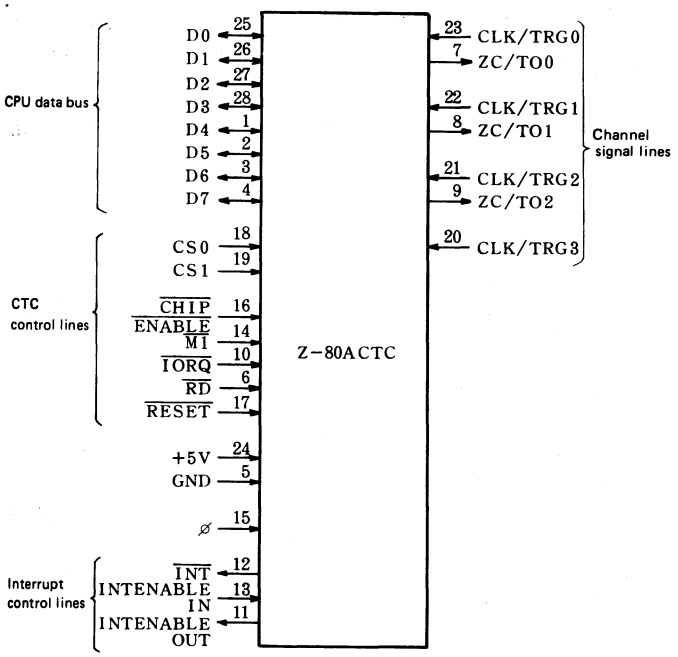


Fig. 61

Z-80CTC pin descriptions

D0-D7: Bidirectional, three-state CPU data bus.

CS0-CS1: Active high channel selector inputs. The CTC creates a two bit binary address code from these selector inputs to select one out of the four independent CTC channels (a truth table is shown below).

	CS1	CS0
Ch0	0	0
Ch1	0	1
Ch2	1	0
Ch3	1	1

CE: Active low chip enable input

Clock(ϕ): System clock input.

M1: Active low input indicating machine cycle 1 from the CPU. If $\overline{M1}$ and $\overline{RD}$ are both active, it indicates the CPU has fetched an instruction from memory. If $\overline{M1}$ and $\overline{IORQ}$ are both active, it indicates the CPU is in an interrupt acknowledge cycle.

$\overline{IORQ}$: Active low I/O request input from the CPU. The $\overline{IORQ}$ is used in conjunction with the $\overline{CE}$ or $\overline{RD}$ when data or channel control words are to be transferred between the CPU and the CTC. During a CTC write cycle, the $\overline{IORQ}$ and $\overline{CE}$ must be both one, and $\overline{RD}$ must be zero. During a CTC read cycle, the $\overline{IORQ}$, $\overline{CE}$, and $\overline{RD}$ must be all active to place the contents of the down counter on the IO data bus. If the $\overline{IORQ}$ and $\overline{M1}$ and both one, it indicates the CPU is in an interrupt acknowledge cycle.

$\overline{RD}$: Active low input indicating CPU read cycle status. The $\overline{RD}$ is used in conjunction with the $\overline{IORQ}$ or $\overline{CE}$ when data or channel control words are to be transferred between the CPU and CTC.

IEI: Active high interrupt enable input. This signal is used to create an interrupt control daisy chain within the system. If there is more than one peripheral device which can be a source of an interrupt within the system, their order of priority is determined by using the IEI and IEO.

IEO: Active high interrupt enable output. This signal is used in conjunction with the IEI, to create a daisy chain used to determine the order of priority of interrupts within the system. The IEO is set high only if the IEI is high, no channel within the CTC is requesting interrupt, and the CPU is not servicing any interrupt from the CTC.

$\overline{INT}$: Open-drain, active-low interrupt request output. This signal goes active if the IEI is high and the down counter on any of the CTC channels which is programmed to enable an interrupt is counted down to zero.

$\overline{RESET}$: Active low reset input.

CLK/TRG3-CLK/TRG0: External clock/timer trigger input with user-selectable active level (high or low). There are four CLK/TRG pins which correspond to the four independent CTC channels. In the counter mode, the counter is decremented by 1 each time an active transition (positive or negative) is applied to this pin. In the timer mode, clock operation is initiated by an active transition applied to this pin.

ZC/TO2-ZC/TO0: Active high zero-count/time-out output. The CTC has three ZC/TO pins which correspond to the CTC channels 2, 1, and 0, respectively (channel 3 has no ZC/TO pin due to package restrictions). In either the counter or timer mode, these pins deliver an active high pulse when the counter has counted down to zero.

14. DISPLAY INTERFACE

14-1 Display interface functions

The MZ-5500 contains a large video RAM space and four integral display control devices to provide more powerful display control features than those available on our conventional MZ and PC series.

(1) Highlights

* Complete bit-map graphic display capacity.
* Integral graphic display controller, μPD7220 controls the display independently of the CPU.
* Resolution available: 640 x 400, 640 x 200, 320 x 400, and 320 x 200 dots.
* Window controller (WDC) provides for up to four multiwindow displays with priority.
* Palette feature plus color priority.
* In color mode, up to eight colors can be specified for each dot; in monochrome mode, up to eight gradations can be specified.
* Up to eight colors or gradations can be specified for the background of windows and borders outside each window (borders are not available on the 400 raster model).
* Large VRAM space of standard 96KB and extended 192KB, which can be accessed from both the CPU and graphic display controller (GDC).

(2) Display specifications

Table 31

		640x400 COLOR	640x400 MONO CHRO	320x400 COLOR	320x400 MONO CHRO
Frames vs. memory size	Standard/ expansion	1 2	3 6	2 4	6 12

Table 32

		640x200 COLOR	640x200 MONO CHRO	320x200 COLOR	320x200 MONO CHRO
Frames vs. memory size	Standard/ expansion	2 4	6 12	4 8	12 24

(3) Usable display type

Table 33

	COLOR	B/W
640 x 400	MZ1D14/ID18	MZ1D13
320 x 400	MZ1D14/ID18	MZ1D13

* Note MZ1D13: 400 raster, 12" green display for the MZ-5600
  MZ1D14: 400 raster, 12" color display for the MZ-5600
  MZ1D18: 400 raster, 15" color display for the MZ-5600
* MZ1D07 or 08 for the MZ-3500 cannot be used.

(4) Synchronization timing

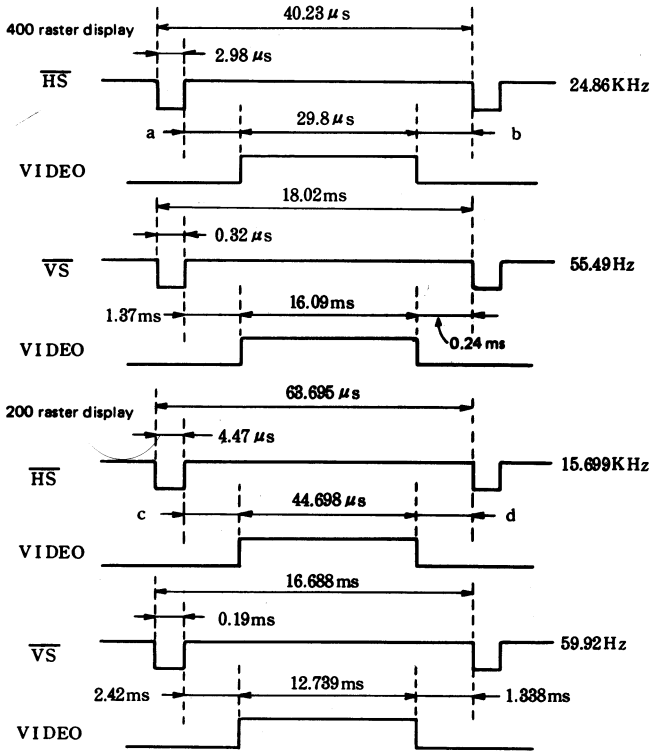


Fig. 64

Table 34

	640 x 400 640 x 200	320 x 400	At the pins of GDC
a	4.85μS	5.03μS	3.73μS
b	2.6 μS	2.42μS	3.73μS

	640 x 200	320 x 200	At the pins of GDC
c	9.5 μS	9.78μS	7.82μS
d	5.03μS	4.75μS	6.70μS

Table 35 CLOCK

	640 x 400	320 x 400	640 x 200	
			MZ1D13 MZ1D14	OTHERS
DOT CK	21.48	10.74	21.48	14.32
2 x CCLK	2.68	2.68	2.68	1.79

	320 x 200	
	MZ1D13 MZ1D14	OTHERS
DOT CK	10.74	7.16
2 x CCLK	2.68	1.79

Unit: MHz

(5) Video RAM configuration

The VRAM consists of dynamic RAM chips of 16K x 4 bits (8KB) each. Its memory map is shown below. The VRAM can be accessed from both the CPU and the graphic display controller (GDC). The CPU accesses it byte-by-byte (8 bits) or word-by-word (16 bits), while the GDC accesses it word-by-word only.

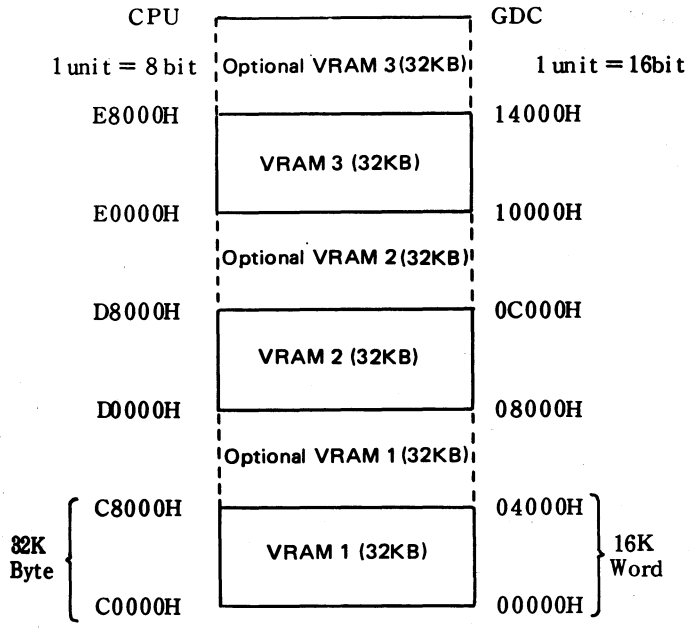


Fig. 65

Display interface logic block diagram

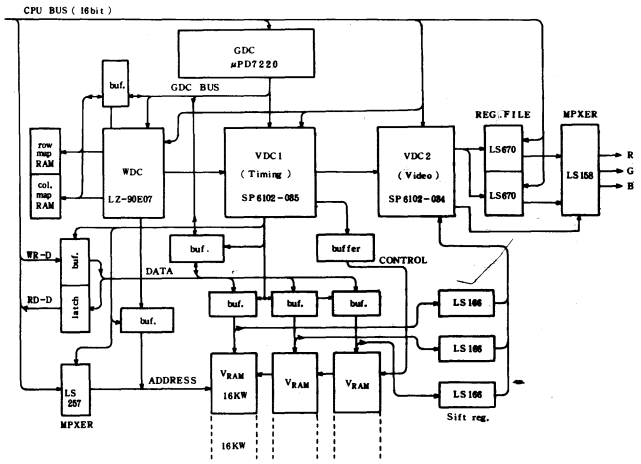


Fig. 66

14-2 Display interface logic description

Display interface logic configuration

The display interface consists of the following chips and blocks:

* Graphic display controller (GDC): μPD7220
* Window controller (WDC): LZ90E07
* Video display controller 1 (VDC1): SP6102-035
* Video display controller 2 (VDC2): SP6102-034
* VRAM: Dynamic RAM
* Mapping RAM (1K x 4 bits): Static RAM
* Palette register file: 74LS670
* Bus buffers and other TTL gates

The display control logic block diagram is shown in Fig. 66.

The display control logic consists of a GDC, WDC, timing generators (VDC1), video signal controller (VDC2), and VRAM. Each block can be accessed from both the CPU and GDC since the display cycle is divided into a CPU cycle and a GDC cycle.

While the CPU treats the GDC as one of the I/O devices, the GDC functions as a sub-processor within the display control logic.

14-3 Logic description

(1) Graphic display controller (GDC: μPD7220)

The GDC is an integral graphic display controller used to control text and graphic information display on a raster scan display screen. It has the following features:

1) Functions and features

* Sync. signal generation: Constantly generates a sync. signal and controls display and drawing timing.
* Preparations for drawing: Calculates drawing addresses based on given command parameters.
* Execution of drawing: Outputs address information to the VRAM to update or correct VRAM data.
* Display: Constantly calculates display addresses and transfers them to the VRAM to read display data.
* Capable of high-speed graphic drawing.
* Direct VRAM control capability.
* Built-in FIFO for I/O interface with the CPU.
* Part of the VRAM area can be displayed.
* Vertical and horizontal scrolling is easy.

Pin configuration

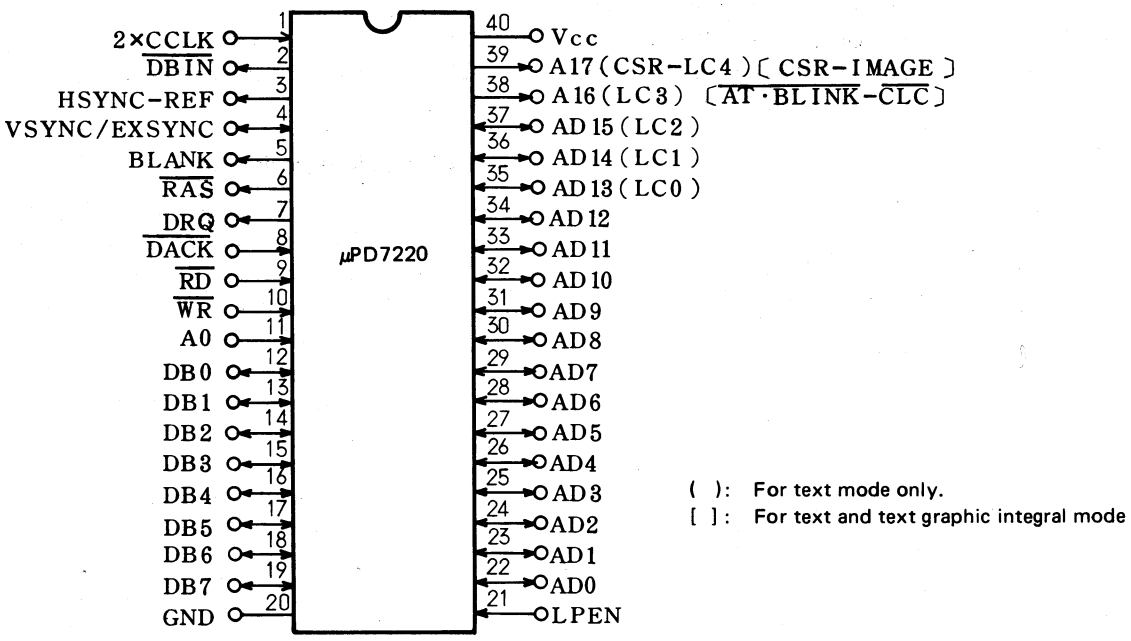


Fig. 67

Block diagram

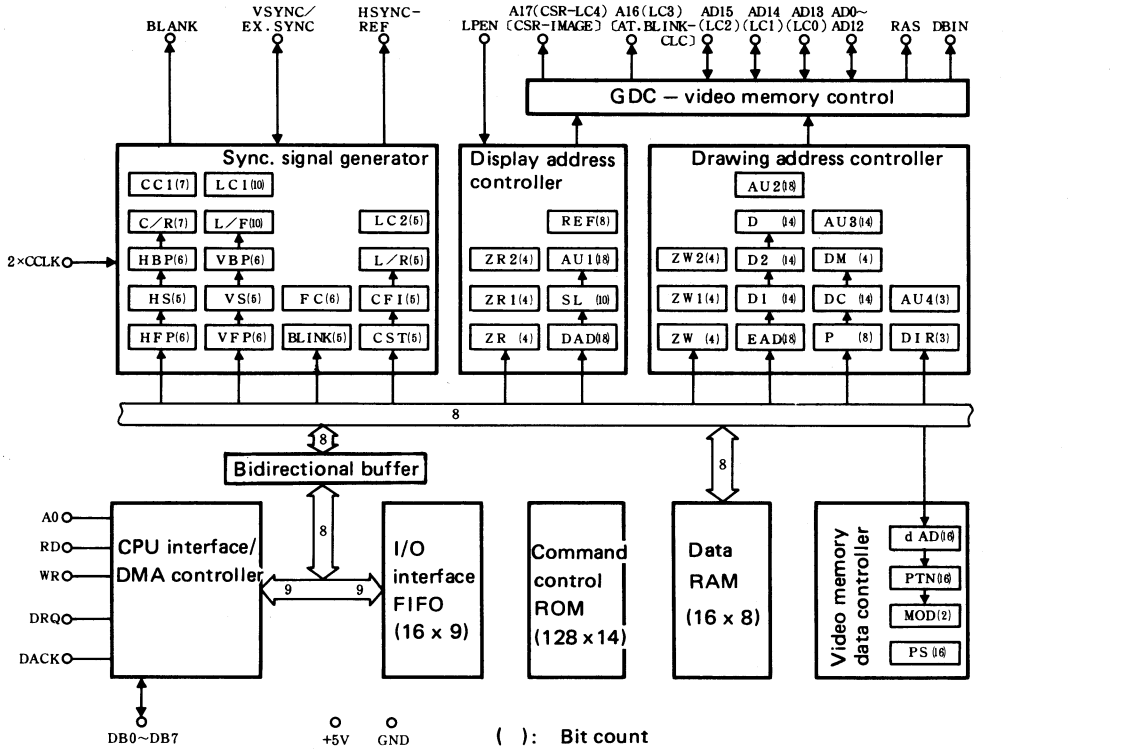


Fig. 68

Pin functions

Table 36

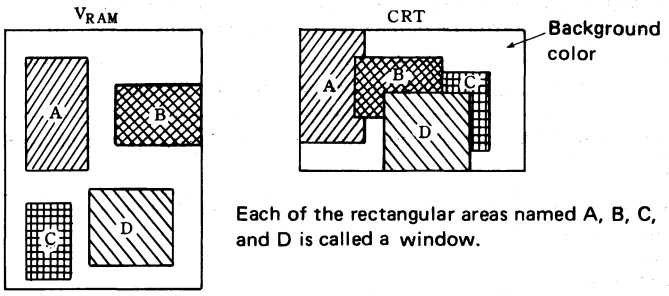
Pin No.	Signal name	IN/OUT	Description
1	2 x CCLK	IN	Accepts a single-phase clock. The clock frequency is determined from the relationship between the number of display characters per row and the horizontal display time. (One clock puls for ever 16 dots (tow charactors))
2	$\overline{DBIN}$	OUT	Output only when accessing the video memory, to place video memory output on the data bus.
3	HSYNC-REF	OUT	Horizontal sync. signal. When the dynamic RAM control mode is selected, this signal may also be used as a refresh timing signal.
4	VSYNC/ EX. SYNC	I/O	May be used in the following two ways depending on whether the GDC is a master or a slave: (1) When the GDC is a master, outputs a vertical sync. signal. (2) When the GDC is a slave, accepts an external sync. signal. (in the MZ5600 system the GDC is always master)
5	BLANK	OUT	Erase signal output used for the following conditions: (1) Horizontal and vertical flyback periods. (2) Between the execution of a display stop command (e.g. RESET or STOP) and that of a START command. (3) During video memory access for read/write.
6	$\overline{RAS}$	OUT	Control signal furnished from the GDC to video memory. In dynamic RAM mode, this is a basic timing for the RAM. When high, functions as an address latch timing signal.
7	DRQ	OUT	DMA request output (not used).
8	DACK	IN	Indicates DMA transfer busy. (Not used)
9	$\overline{RD}$	IN	Accepts a low level signal when the CPU wants to read data or status flag out of the GDC.
10	$\overline{WR}$	IN	The CPU turns this input to low when it wants to write a command or parameter into the GDC.
11	A0	IN	Normally the least significant bit of the CPU address bus is connected to this pin, to specify data types.
12 ~ 19	DB0 ~ DB7	I/O	Bidirectional data bus.
20	GND	IN	0V return line.
21	LPEN	IN	Accepts a high level when the light pen senses an optical input. At this time, the CPU can read the display address latched in the GDC by using the LPEN command.
22 ~ 37	AD0 ~ AD15	IN	Bidirectional address/data bus connected to the video memory. During memory refresh, refresh address is output on the low order 8 bits of this bus. In the text mode the AD13 ~ AD15 are sued as a line count output.
38 39	AD16, AD17	OUT	Video memory address output.
40	V_{CC}	IN	+5V power supply.

A0	$\overline{RD}$	$\overline{WR}$	Function
0	0	1	Read status flag.
1	0	1	Read data.
0	1	0	Write parameter.
1	1	0	Write command.

(2) Window controller (WDC)

Outline of WDC function

The WDC is used to display a certain rectangular area on the VRAM onto arbitrary locations on the display screen, as shown in the following figure:



Each of the rectangular areas named A, B, C, and D is called a window.

Fig. 69

Features of WDC

1) Up to four windows can be displayed at a time.
2) The order of priority can be specified for each window, so that each window may be overlapped according to the order of priority.
3) When there are three VRAM planes, each of these planes can be displayed, or two or three planes may be overlapped on each other.
4) Input address may be directly output without using the window feature.

WDC block diagram

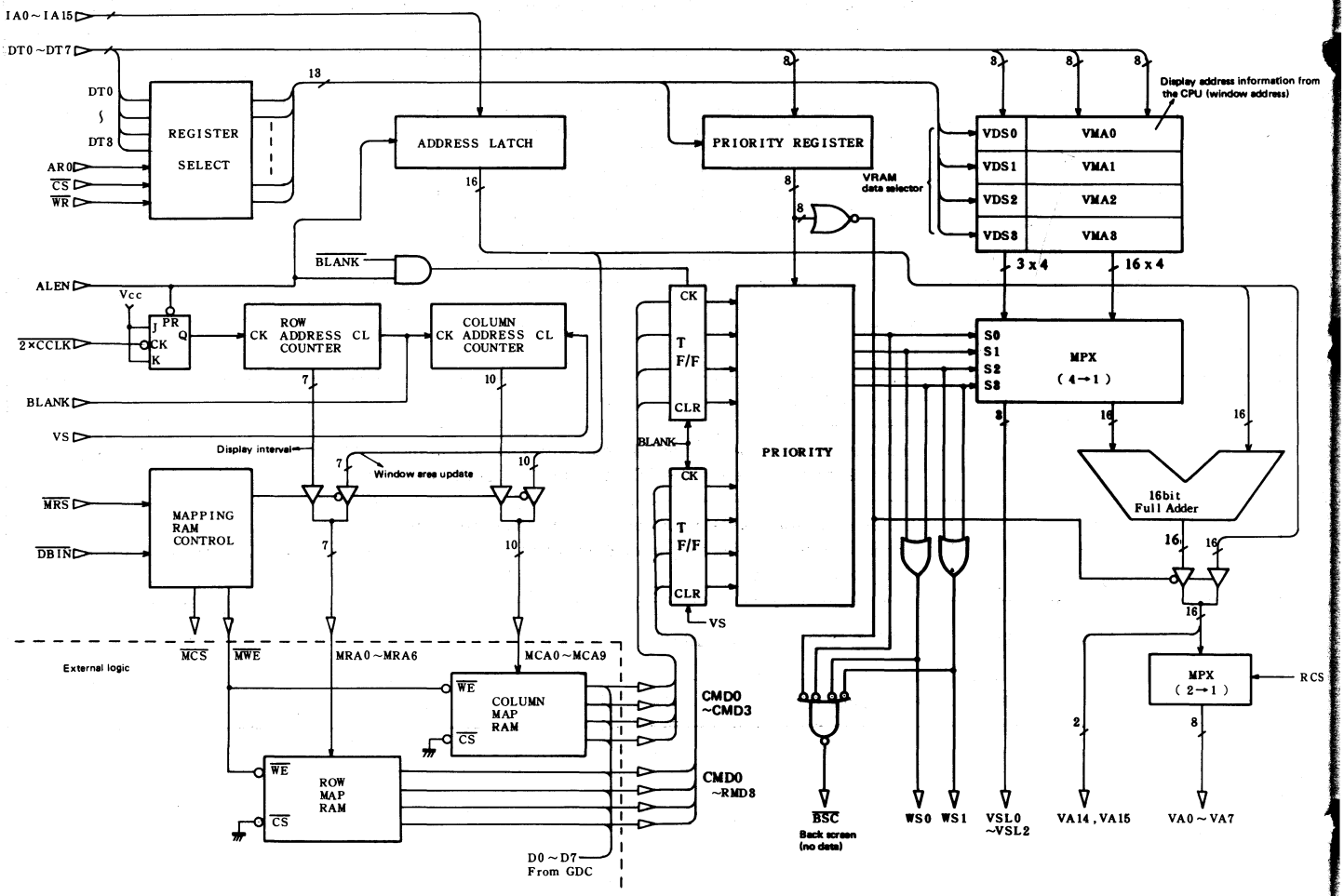


Fig. 70

WDC (LZ-90E07) pin functions

Table 37

Pin No.	Signal name	IN/OUT	Description
1 ~ 8	VA0 ~ VA7	OUT	V_{RAM} address output, which is a multiplex of row and column addresses. (V_{RAM} address)
9	RCS	IN	Intra-chip multiplexer switching signal (row or column selector).
10	GND	IN	0V input
11	VA14	OUT	V_{RAM} address output
12	VA15	OUT	V_{RAM} address output
13 ~ 16	RMD0 ~ RMD3	IN	Data input from row address mapping RAM (row address mapping data).
17 ~ 20	CMD0 ~ CMD3	IN	Data input from column address mapping RAM (column address mapping data).
21	$\overline{MCS}$	OUT	Data bus buffer gate signal for mapping RAM.
22	$\overline{MWE}$	OUT	Mapping RAM write enable (mapping RAM write enable)
23 ~ 29	MRA0 ~ MRA6	OUT	Address bus output to row address mapping RAM (mapping RAM row addresses 0–6).
30 ~ 39	MCA0 ~ MCA9	OUT	Address bus output for column address mapping RAM (mapping RAM column addresses 0–9).
40	$\overline{CS}$	IN	Internal register chip selector input.
41	$\overline{WR}$	IN	Internal register write input.
42	$\overline{MRS}$	IN	Mapping RAM control logic selector (mapping RAM control circuit select).
43 ~ 60	IA0 ~ IA15	IN	Address bus input (input address 0–15).
61	$\overline{2XCCLK}$	IN	Trigger input (display clock). Used increment to ROW address counter.
62	BLANK	IN	Blank signal input from μPD7220, used to clear the row address counter for the mapping RAM and as a clock input to the column address counter.
63	VS	IN	Vsync. signal input from μPD7220, used to clear the column address counter for the mapping RAM
64	ALEN	IN	Address latch enable input.
65	$\overline{DBIN}$	IN	$\overline{DBIN}$ input from μPD7220, used for the GDC, in conjunction with the $\overline{MRS}$, to access the mapping RAM.
66	AR0	IN	Internal register select logic (RNO) address (A1) input.
67 ~ 74	DT0 ~ DT7	IN	Data bus input
75 ~ 77	VSL0 ~ VSL2	OUT	V_{RAM} data output select signal (V_{RAM} select 0–2) (For more details see the description of VDC2 LSI.)
78 79	WS0 WS1	OUT	Window select signals, used, in conjunction with the VSL0–2 signals, to control the V_{RAM} output (window select 0–1).
80	$\overline{BSC}$	OUT	Border color output (back screen). (For more details see the decription of VDC2 LSI.)

(3) Mapping RAM

Outline

* The mapping RAM is used to specify the location and area occupied by each window on the display screen.
* The mapping RAM exists on the GDC's memory map, as shown in the above figure (can not accessed from the CPU).
* The mapping RAM is used in correlation with the display screen, as illustrated below (for 640 x 400 dot display):

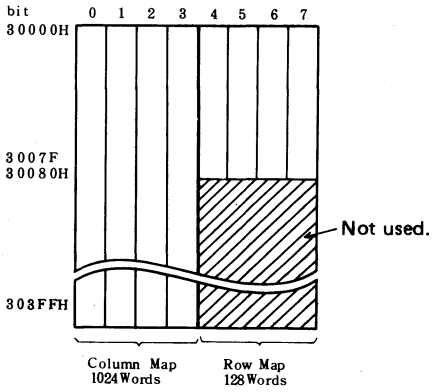


Fig. 71

Mapping RAM access

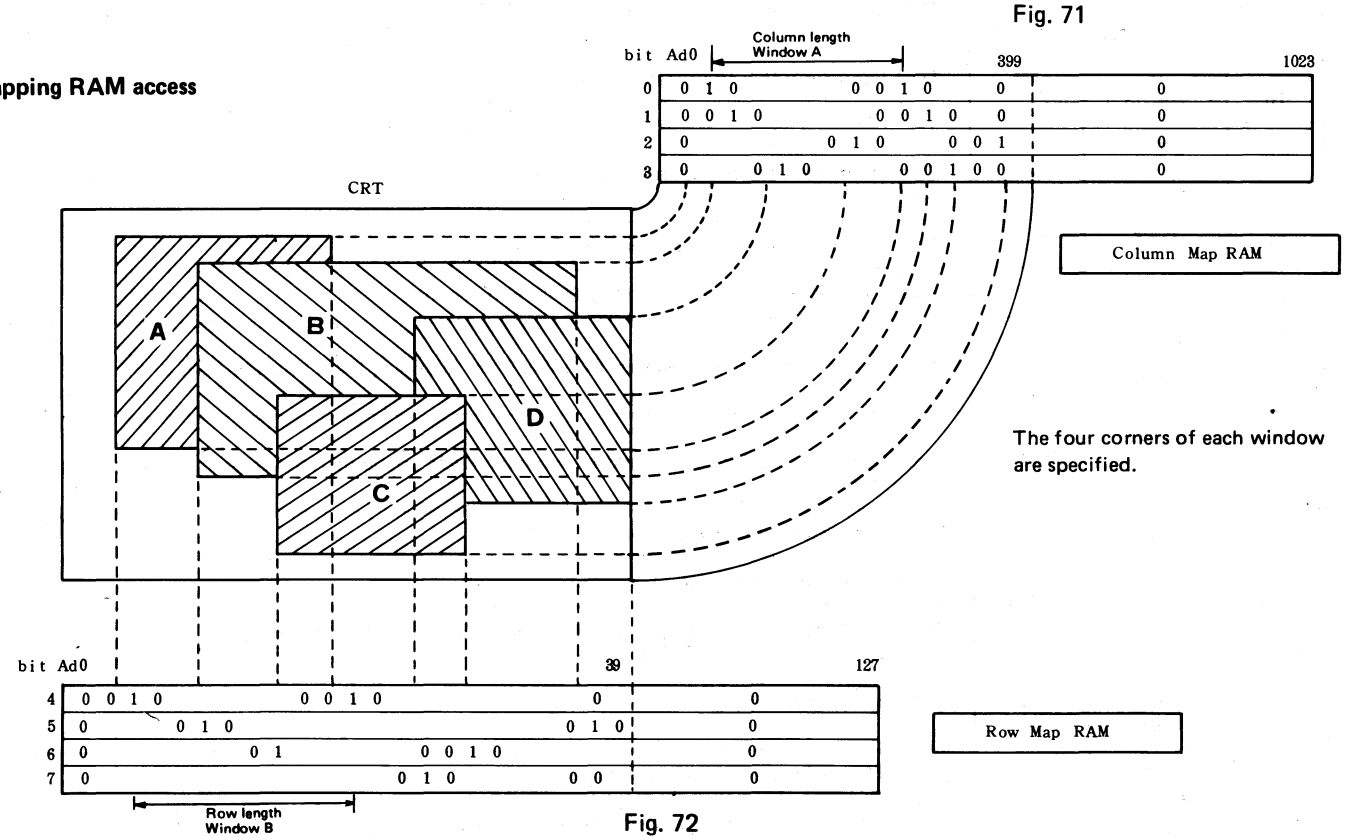


Fig. 72

* Mapping information is divided into horizontal and vertical components when written into the mapping RAM, as shown above.
* As each window is located using 4 bits, no more than 16 bits are ever set at any one time.
* Initial information is written into the mapping RAM by using the GDC's drawing feature.

Configuration of WDC and mapping RAM

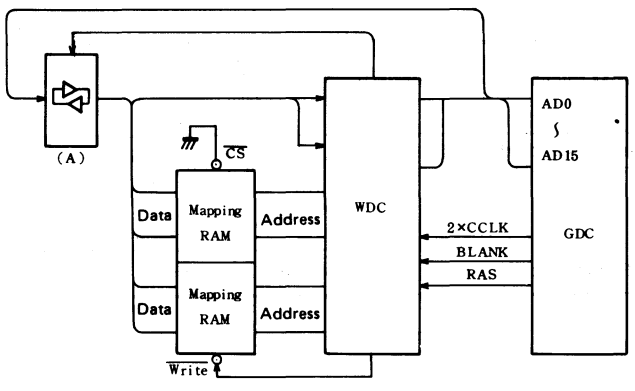


Fig. 73

The Fig, 73 provides the WDC, mapping RAM, and GDC configuration. The $\overline{CS}$ of the mapping RAM is always low, and is read when windows are displayed. When writing data into the mapping RAM, the WDC controls the buffer (A) and RAM write signal to let the GDC write the necessary data.

Fig. 70 shows the WDC block diagram. The WDC latches address information (for displaying, drawing and refreshing) transferred from the GDC, and modifies it according to the contents of the VMA or mapping RAM, if needed.

The WDC knows the locations of windows from bit information read out of the mapping RAM, latches the display address transferred from the GDC, adds VMA to the latched display address, and uses the resulting address as the actual display address on the screen. However, when the GDC is blanking (for drawing or refreshing) or if the priority register value is zero, the WDC directly outputs the display address which has been transferred from the GDC.

(4) VDC1 (SP6102-035)

VDC1 functional outline

* Produces the DCK (dot clock) by halving 3 master clocks for 400 rasters (CK0), 200 rasters (CK1) and superimposing (CK2). The 2XCCK (GDC clock) is produced by dividing the above master clocks by 16.
* Generates the RAS0-RAS5, CAS, and bidirectional buffer gate signals $\overline{VDE0}$-$\overline{VDE2}$, which are used by the CPU or GDC to access the VRAM.
* Produces display timing control signals.

VDC1 (timing control) block diagram

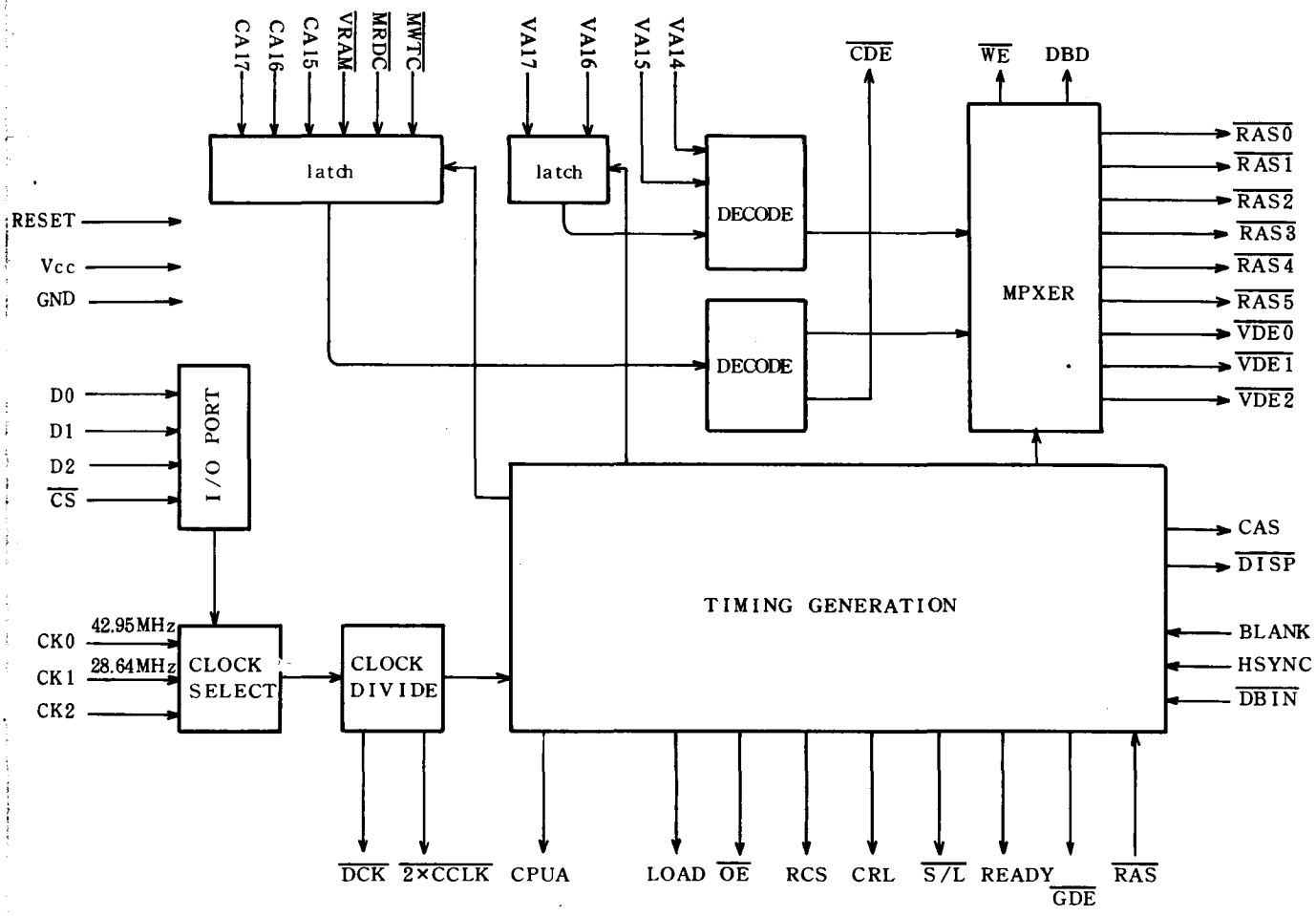


Fig. 74

VDC1 (SP6102-035) pin functions

Table 38

Pin No.	Signal name	IN/OUT	Description
1 ~ 6	$\overline{RAS0}$ ~ $\overline{RAS5}$	OUT	Row address select ($\overline{RAS}$) signal for the V_{RAM}. During CPU access timing, the $\overline{RAS}$ of the accessed RAM is set low. During display timing, $\overline{RAS0}$, 2, 4, or $\overline{RAS1}$, 3, 5 are set low. During RAM refresh, RAS0–5 are all set low.
7 8 9	CK0 CK1 CK2	IN IN IN	Clock input for 400 rasters. Clock input for 200 rasters. External clock input (from SPCK).
10	OE	OUT	V_{RAM} output enable. Since the CPU performs advanced writes to the V_{RAM}, the $\overline{OE}$ remains at low.
11	$\overline{WE}$	OUT	V_{RAM} write enable.
12	CAS	OUT	V_{RAM} column address select (CAS) signal. The $\overline{CASH}$ and $\overline{CASL}$ signals are created from this CAS signal.
13	GND	IN	0V input
14	$\overline{DISP}$	OUT	Switches the $\overline{CASH}$ and $\overline{CASL}$ signals for CPU access and GDC access. Also used as a latch timing signal (CCAS) for the BHE and A0.
15 ~ 17	$\overline{VDE0}$ ~ $\overline{VED2}$	OUT	V_{RAM} data bus buffer enable.
18	$\overline{GDE}$	OUT	GDC data enable.
19	$\overline{CDE}$	OUT	CPU data enable.
20	READY	OUT	XACK output to the CPU.
21	RCS	OUT	V_{RAM} row and column address select signal (input to the S pin of MPX).
22	RESET	IN	Reset input
23 ~ 26	VA14 ~ VA17	IN	V_{RAM} address input from the WDC or the GDC.
27	$\overline{2XCCLK}$	OUT	GDC clock output
28	HS	IN	HSYNC input from the GDC
29	BLANK	IN	BLANK input from GDC.
30	$\overline{RAS}$	IN	Row address select (RAS) input from the GDC.
31	$\overline{DBIN}$	IN	Data bus in (DBIN) input from the GDC.
32	DBD	OUT	Direction select signal for bidirectional data bus buffer. High for V_{RAM} read; low for V_{RAM} write (Data bus direction).
33	CRL	OUT	CPU read latch clock used to read V_{RAM} data into the CPU.
34	CPUA	OUT	Switches address buffers for CPU access and GDC access (for diaplaying, refreshing or drawing). High for the CPU; low for the GDC.
35	LOAD	OUT	Load signal for VDC2 LSI
36	V_{CC}	IN	+5V power supply
37	$\overline{DCK}$	OUT	Display dot clock
38	S/L	OUT	Shift/load signal for the P/S conversion IC (LS166).
39	$\overline{CS}$	IN	Chip select input.
40	$\overline{V_{RAM}}$	IN	$\overline{V_{RAM}}$ chip select.
41	$\overline{MWTC}$	IN	Memory write control ($\overline{MWTC}$) from the CPU.
42	$\overline{MRDC}$	IN	Memory read control ($\overline{MRDC}$) from the CPU.
43 ~ 45	CA15 ~ CA17	IN	Address input A15–A17 from the CPU.
46 ~ 48	D0 ~ D2	IN	Data input from CPU.

Internal VDC1 configuration

* Clock inputs

One of the three clocks, CK0, CK1, and CK2, is selected with the D0 and D1 on the I/O port, and is halved.

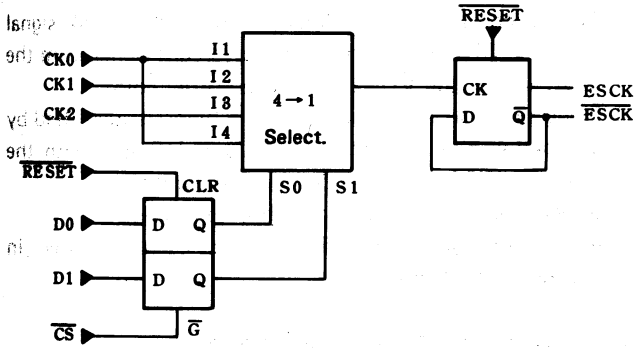


Fig. 75

* Dot clock and 2xCCLK outputs

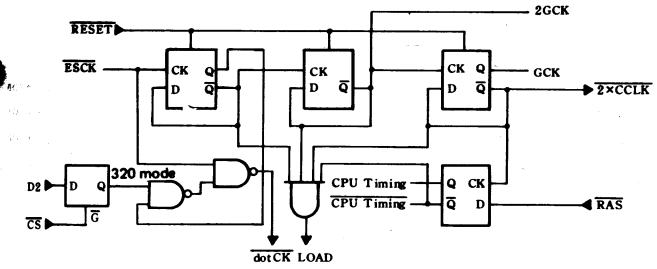


Fig. 76

The 2xCCLK is obtained from dividing the ESCK by 8. The dot clock is switched by the I/O port D2, for the 320 dot mode.

* RAS and CAS

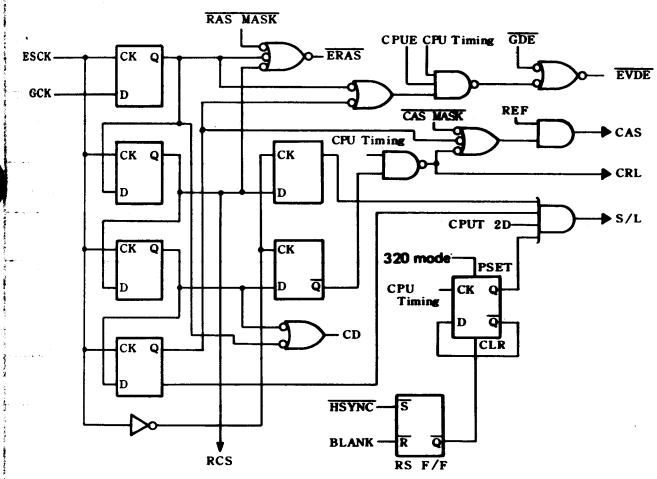


Fig. 77

The RAS and CAS signals are created from the 2xCCLK, by delaying it and then gating it. In the 320 dot mode, the Shift/load (S/L) is added each time.

* ERAS: RAS0-5 are created from ERAS.
* EVDE: VDE0-2 are created from EVDE.
* RASMASK, CASMASK: Prevents RAS and CAS from being set high while the GDC is drawing.
* REF: Prevents CAS from becoming active during VRAM refresh.

* CPUT 2D: CPU timing delayed by 2X dot clocks.
* CD: CDE is created from CD.

* OE

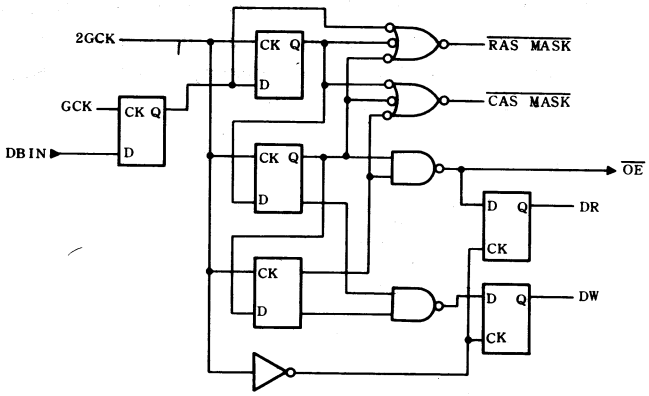


Fig. 78

The OE is created from the latched DBIN, so it may be set high only while the GDC is drawing.

* DR: Data read by the GDC from VRAM.
* DW: Data written by the GDC into VRAM.

* CPUA

The CPUA is created by halving the ERAS.

* DISP

The DISP is created by delaying the CPU timing by twice the ESCK period.

* GDE

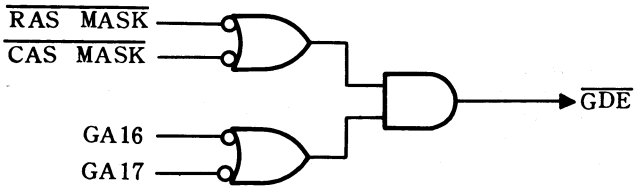


Fig. 79

The GDE is the GDC's drawing address. If both A16 and A17 are high, the GDE, is not set low since the mapping RAM area is addressed.

* PAS0-6, VDE0-2, WE, DB0

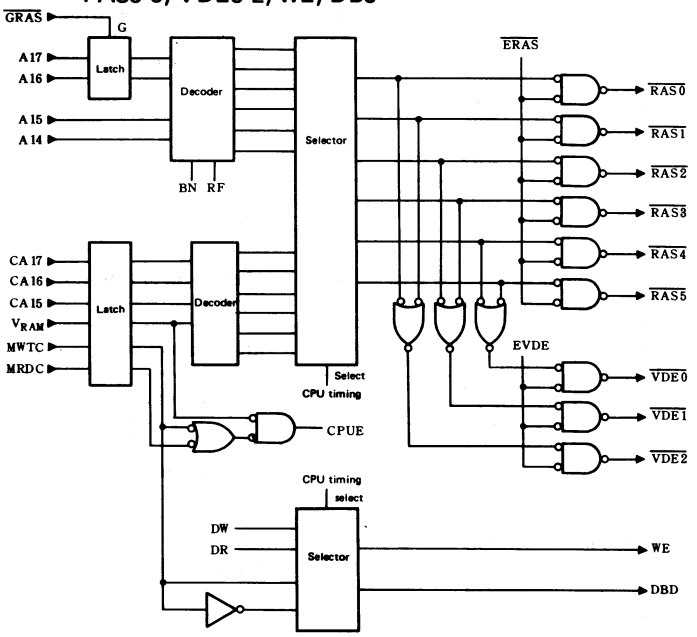


Fig. 80

CPU commands and addresses are latched within the VDC1. Display addresses DA14 and DA15 are latched within the WDC, and are not latched into the VDC1. The decoder (DA14-17) also accepts refresh (RF) and blank (BN) inputs. During refresh, the decoder activates all the chip selectors. During display, it activates RAS0, 2, 4 or RAS1, 3, 5 by using the DA14.

* $\overline{CDE}$

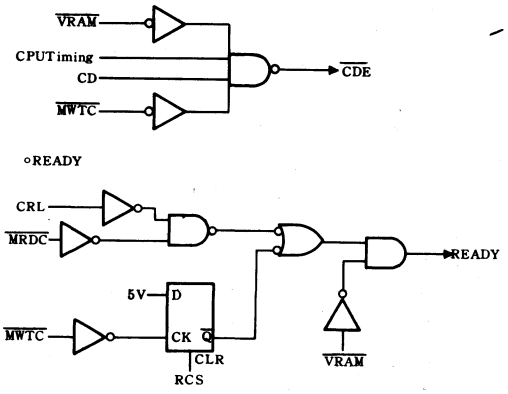


Fig. 81

(5) VDC2 (SP6102-034) -- Video composition

VDC2 functional outline

a) Background color — If data is all zeros, the VDC2 provides background color for the window according to the window number.

b) Border color — If the logical OR of the Blank signal from the GDC and the BSC (back screen) signal from the WDC is true, the VDC2 outputs a border color.

c) Plane priority — The priority of a plane is identified by comparing the data in VRAM1 and VRAM2 with the value set on the I/O port by the comparator.

d) Superimposition in the monochrome mode —

e) Normal/reverse video display for each window, in monochrome mode.

VDC2 (video composition) block diagram

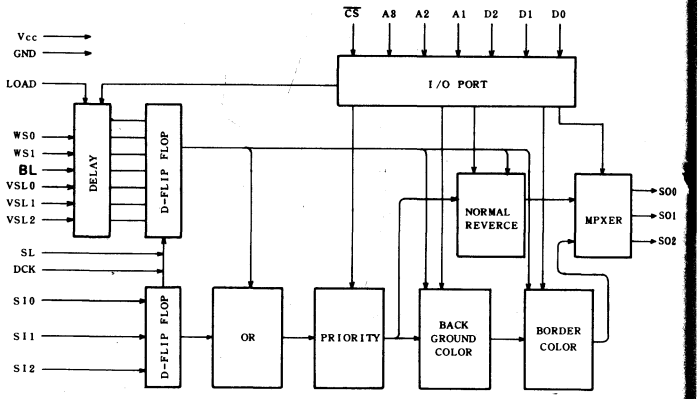


Fig. 82

Table 39 **VDC2 (SP6102-034) pin functions**

Pin No.	Signal name	IN/OUT	Description
1 2	WS0 WS1	IN	Window select signal from WDC
3 ~ 5	VSL0 ~ VSL2	IN	V_{RAM} data select input from the WDC.
6	LOAD	IN	Used to latch the HSYNC and BLANK signals from GDC, and the VSL0—2, WS0, 1, and BSC signals from the WDC.
7	S/L	IN	Shift load input (from SP6102—035).
8	DCK	IN	Dot clock input (from SP6012—035).
9 ~ 11	SO0 ~ SO2	OUT	Serial data output to palet resistor
12	GND	IN	0V input
13 ~ 15	Si0 ~ Si2	IN	Display data from the P/S converter (74166) input (serial).
16	BLNK	IN	Blank signal input.
17	$\overline{CS}$	IN	Chip select input.
18 ~ 20	A1 ~ A3	IN	Address bus from the CPU.
21 ~ 23	D0 ~ D2	IN	Data bus from the CPU.
24	V_{CC}	IN	5V

Internal VDC2 configuration

* Display data output from the shift register has a delay of one display cycle plus four dot clocks with respect to the GDC cycle. Therefore, other signals are also delayed by using the following logic:

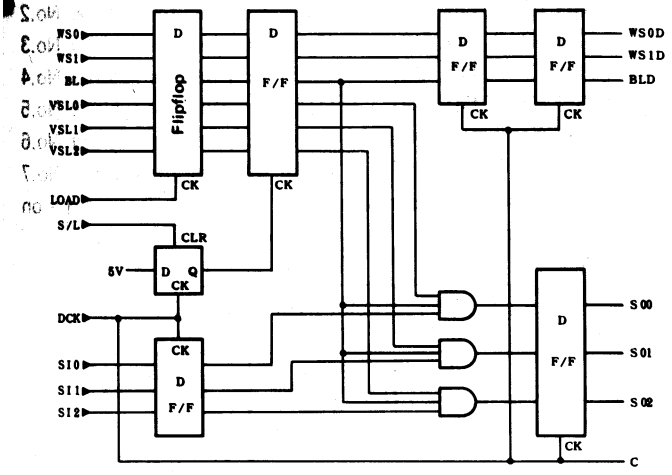


Fig. 83

Input data is combined (AND) with VSL0-2 and BL, and is timed by a type-D flipflop. The WS0, WS1, and BL are delayed further by two clock timings to provide background and border colors.

* Plane priority logic

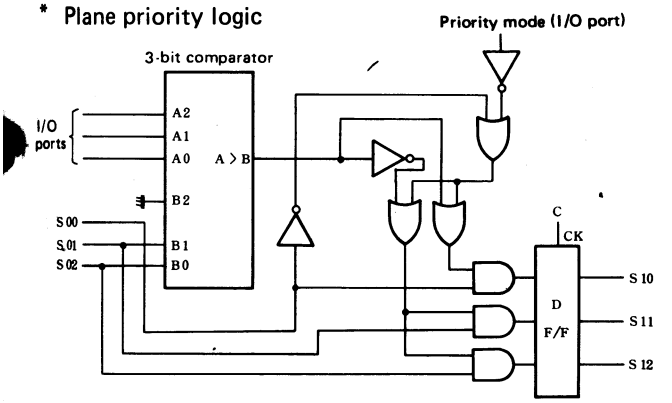


Fig. 84

* Background color

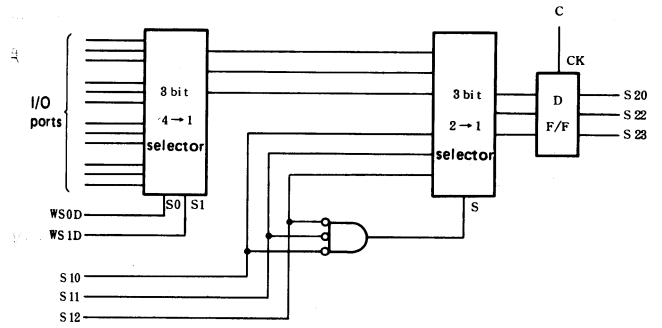


Fig. 85

Background color data furnished to the I/O port is output when the display data is all zeros. Data from the I/O port is switched for each window using WS0-2.

* Monochrome mode reverse video logic

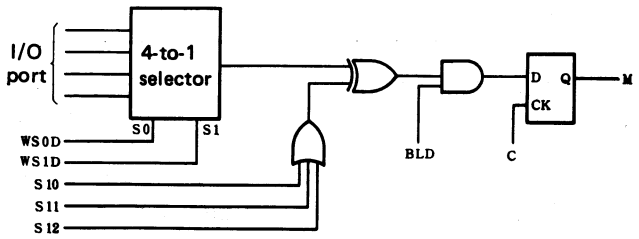


Fig. 86

In the monochrome mode, three pieces of display data are combined (OR). Reverse video is accomplished on the data on the I/O port selected by WS0 and 1. To prevent the border area from being reversed, the display data is combined (AND) with the Blank signal.

* Output logic

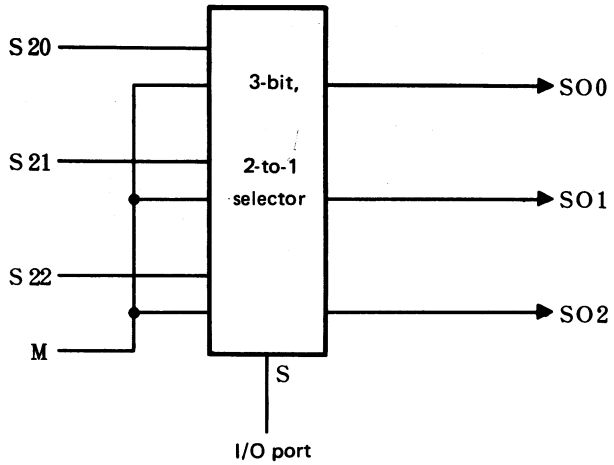


Fig. 87

(6) Register File (RFL) 74LS670

The palette feature is provided by the 74LS670. The 74LS670 is a 4 x 4 bit high-speed static RAM. Two chips are used to provide 8 x 4 bits RAM space, of which 8 x 3 bits are used for the palette feature.

The read output is always enabled, and the address input accepts the address information furnished by VDC2. The color actually displayed is determined by the data written from the CPU into the 74LS670.

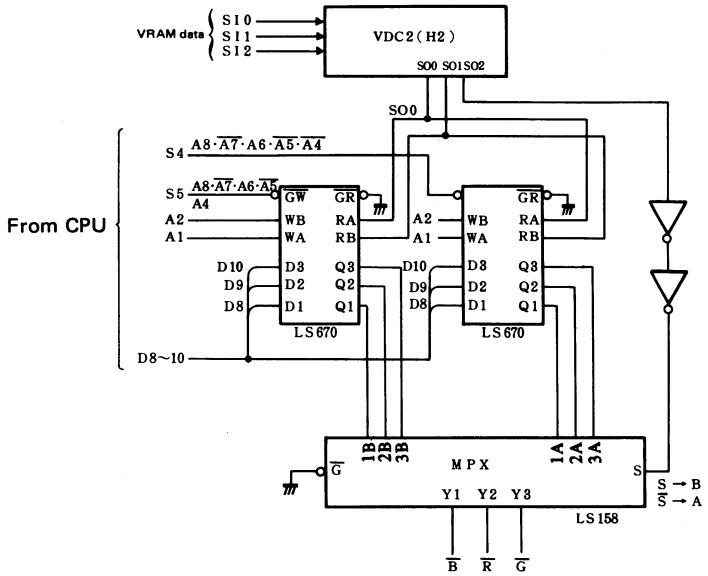


Fig. 88

74LS670 write function table

Table 40

Write input			Word			
WB	WA	GW	0	1	2	3
L	L	L	Q = D	QO	QO	QO
L	H	L	QO	Q = D	QO	QO
H	L	L	QO	QO	Q = D	QO
H	H	L	QO	QO	QO	Q = D
X	X	H	QO	QO	QO	QO

74LS670 read function table

Table 41

Read input			Output			
RB	RA	GR	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

Notes: 1) H: High level, L: Low level, X: Optional level, Z: High impedance (off).

2) Q=D: Selected internal flipflop's output, assuming that data is input to all the four external data inputs.

3) QO: Level of Q before the input condition is established.

4) W0B1: Bit 1 of word 0, and so on.

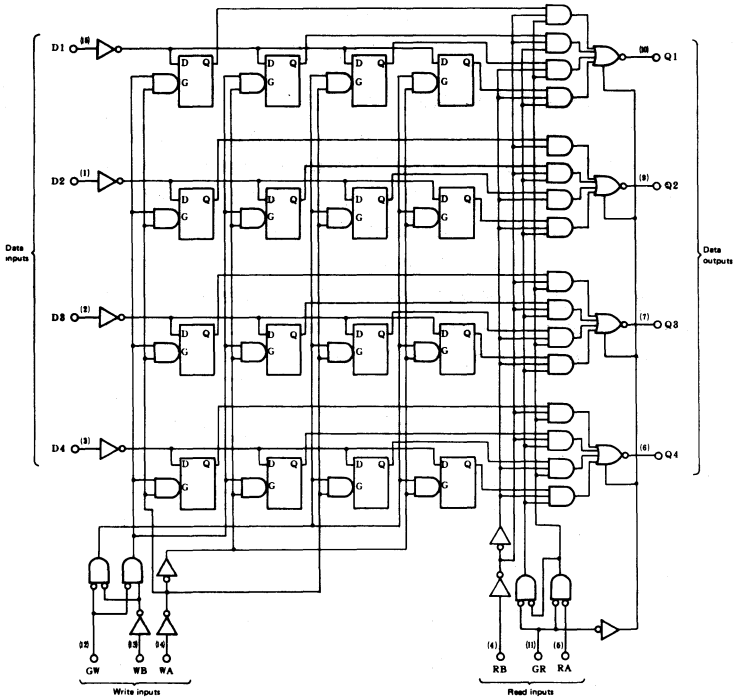


Fig. 89

Colors on a color display and gradations on a monochrome display are specified by values set in the palette register (74LS670).

Data loaded in the VRAM is simultaneously read through VRAM 1, 2, and 3 for the display. These three bits, if regarded as binary numbers, represent decimal numbers 0 through 7, which are used to define palette numbers. Which color is assigned to each palette number depends on the following color numbers set in palette registers:

141H (D10, D9, D8) . . Color number for register No.0
143H (D10, D9, D8) . . Color number for register No.1
145H (D10, D9, D8) . . Color number for register No.2
147H (D10, D9, D8) . . Color number for register No.3
151H (D10, D9, D8) . . Color number for register No.4
153H (D10, D9, D8) . . Color number for register No.5
155H (D10, D9, D8) . . Color number for register No.6
157H (D10, D9, D8) . . Color number for register No.7

The color numbers correspond to the colors (gradations on a monochrome display) listed in the following table:

Table 42

CRT Color No.	Color (RGB), Color	Monochrome, Gradation
0	Black	Black
1	Blue	7
2	Red	6
3	Magenta	5
4	Green	4
5	Cyan	3
6	Yellow	2
7	White	1

(7) Display logic chip selector

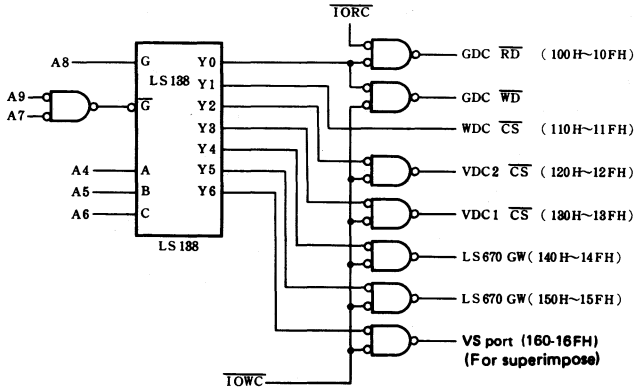


Fig. 90

As showns above, chip selection is accomplished by an LS138 chip. The chip select outputs are gated with the IOWC and IORC.

* VRAM area decoder

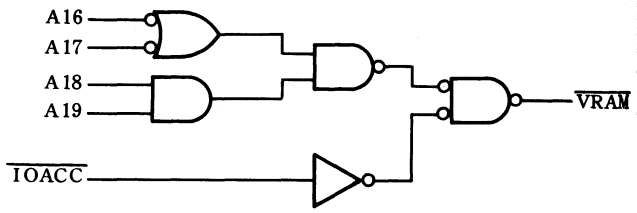


Fig. 91

The VRAM output is set low when the VRAM occupies an area of C0000H through EFFFFH.

(8) VRAM bus control

(i) VRAM bus cycle

VRAM bus cycle is divided into GDC and CPU cycles, as shown below. The CPU timing signal (VDC1 internal signal) samples the RAS (GDC) at the trailing edge of the 2xCCLK signal.

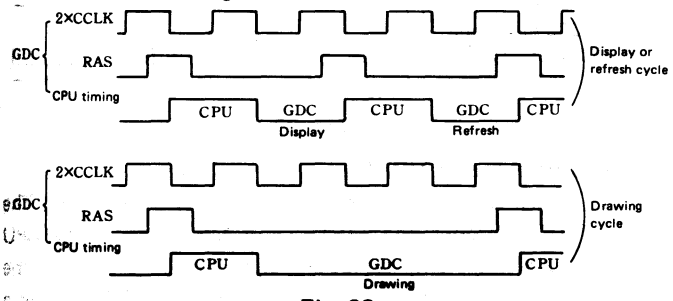


Fig. 92

The VRAM can be accessed from the CPU when the CPU timing is high, and can be accessed from the GDC when it is low.

(ii) VRAM data bus

The following figure provides the VRAM data bus logic.

1) During display or RAM refresh cycle, the $\overline{\text{VDE0-2}}$, $\overline{\text{GDE}}$, and $\overline{\text{CDE}}$ are all high, leaving the bus buffer outputs off.
2) For reading access from the CPU, the pertinent $\overline{\text{VDE}}$ is set low and the CRL of the LS374 is set high, to latch read data.
3) For writing access from the CPU, the $\overline{\text{CDE}}$ and the corresponding $\overline{\text{VDE}}$ are set low.
4) For drawing access from the GDC, the $\overline{\text{GDE}}$ and corresponding $\overline{\text{VDE}}$ are set low. However, if A16 and A17 of the GDC are both one, the $\overline{\text{GDE}}$ remains at high since the mapping RAM area is accessed. The DBD is normally a RAM read line, and is turned into a RAM write line only when accessed from the CPU or GDC.

If the reset line for VDC1 is set low, the $\overline{\text{GDE}}$, $\overline{\text{CDE}}$, and $\overline{\text{VDE0-2}}$ are all set high.

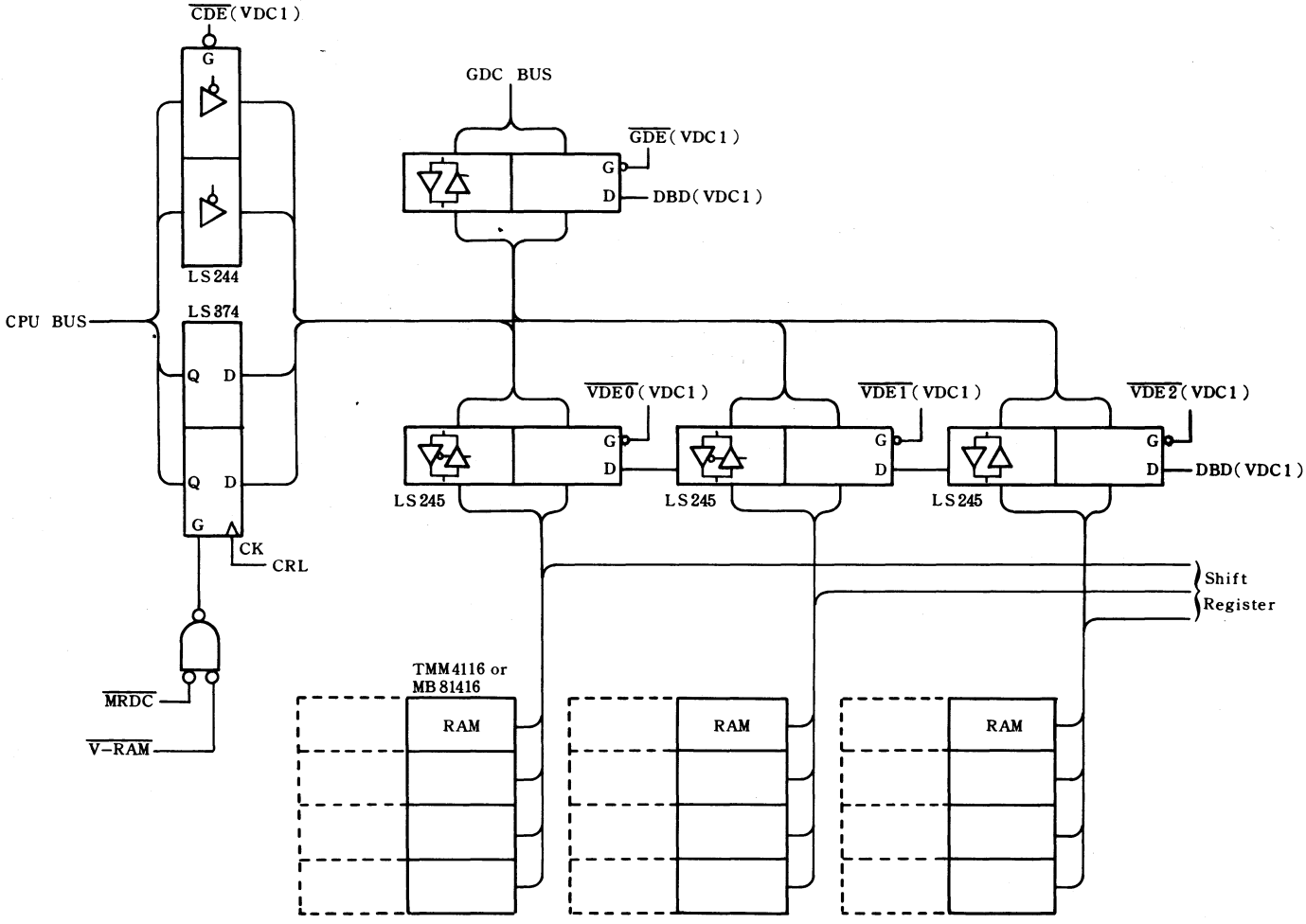


Fig. 93

(iii) VRAM timing

The following shows various VRAM timings:

* Display and refresh timings

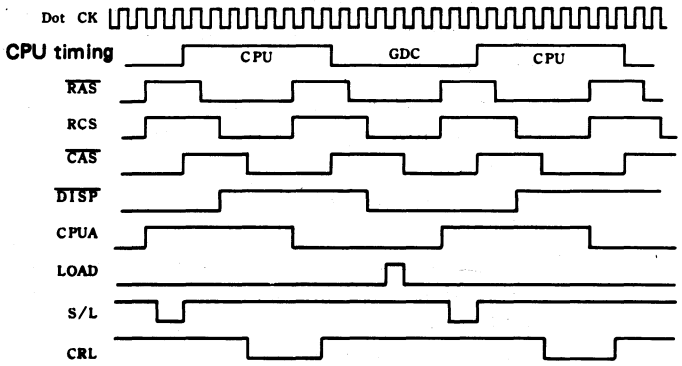


Fig. 94

* Drawing timing

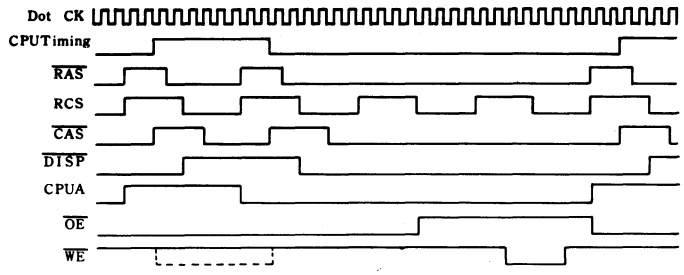


Fig. 95

(iv) VRAM address bus

VRAM address is created by the following logic:

1) The CPU address or the GDC address is selected setting either output to a high impedance using the CPUA signal (high for CPU, low for GDC).
2) Switching between row and column addresses is accomplished by the LS257 for the CPU, and within the WDC chip for the GDC, both using the RCS signal (RCS high for A1–A8, low for A9–A14).

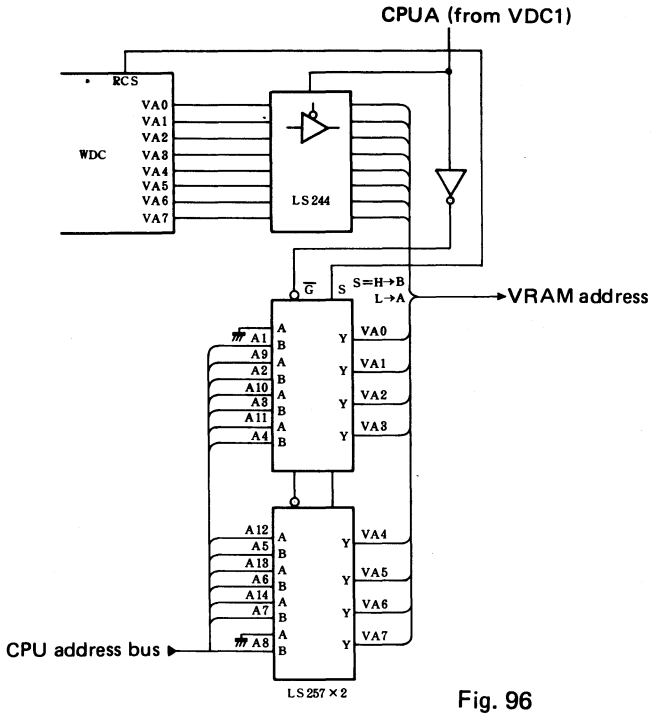


Fig. 96

(v) Shift register clock

In the 320 dot mode, the internal VDC1 clock is obtained by halving the Dot CK S/L for the 640 dot mode, as shown below:

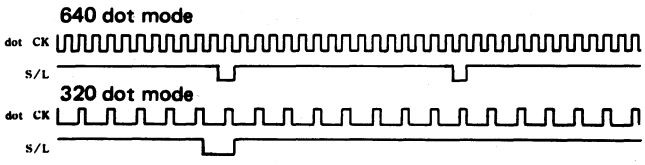


Fig. 97

(vi) CPU access to VRAM

The CPU is clocked asynchronously with the GDC. The VDC1 latches the $\overline{\text{MRDC}}$ and $\overline{\text{MWTC}}$ from the CPU and $\overline{\text{VRAM}}$ chip select signal VRAM into itself at the leading edge of a timing available to the CPU. When a valid command is transferred from the CPU, the VDC1 performs a read or write operation to the VRAM and, at the same time, returns a READY to the CPU.

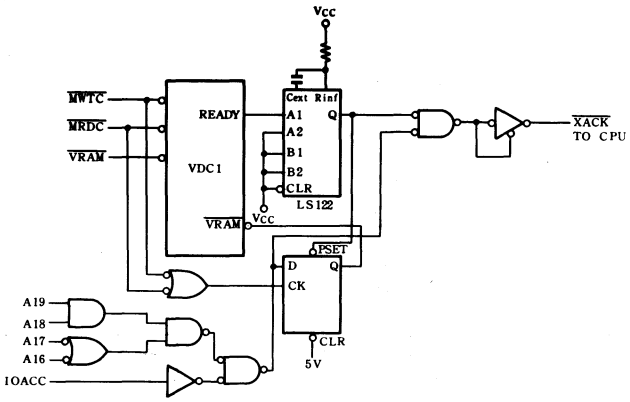


Fig. 98

* The $\overline{\text{VRAM}}$ output is set low when the CPU address is C0000H to EFFFFH.
* A monostable multivibrator is triggered by the trailing edge of the READY signal to create the $\overline{\text{XACK}}$ signal with a pulse width of approximately 200ns.

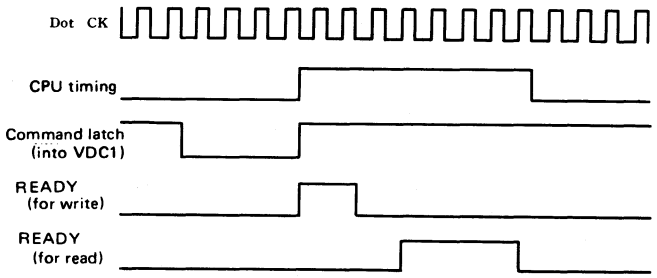


Fig. 99

(9) Display signal output logic

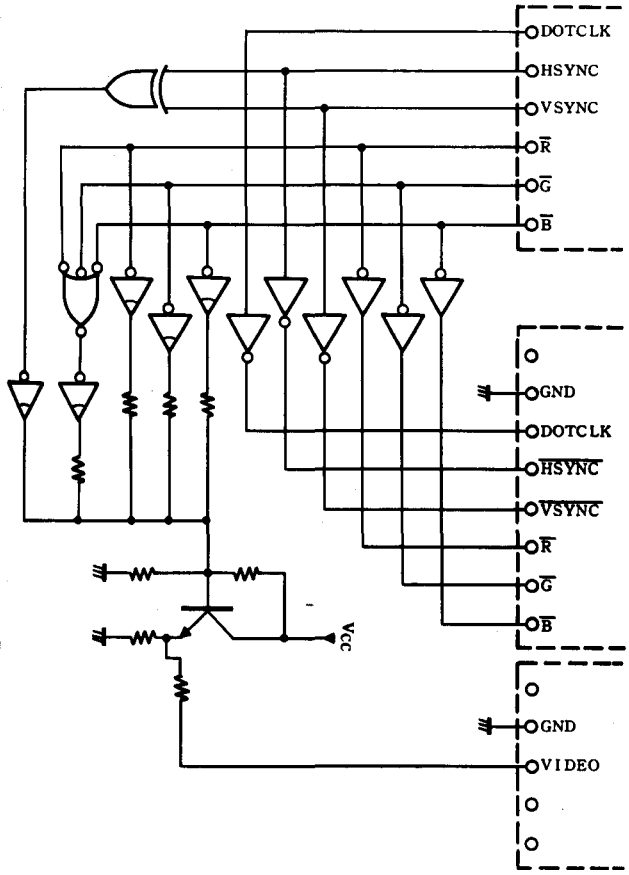


Fig. 100

The above logic is contained in the CPU PWB, and is used to interface the display data output of the CPU PWB with the display.

* For a display with RGB inputs, the interface directly outputs the R (red), G (green), B (blue), $\overline{\text{HSYNC}}$ (horizontal sync.), $\overline{\text{VSYNC}}$ (vertical sync.), and DOTCLK (dot clock) to the display via buffers.
* For a monochrome display, the interface synthesizes the video signals (R, G, B) with the sync. signals (HSYNC, VSYNC), providing D/A conversion on the resulting signal, and outputs it as a monochrome video signal via an emitter follower.

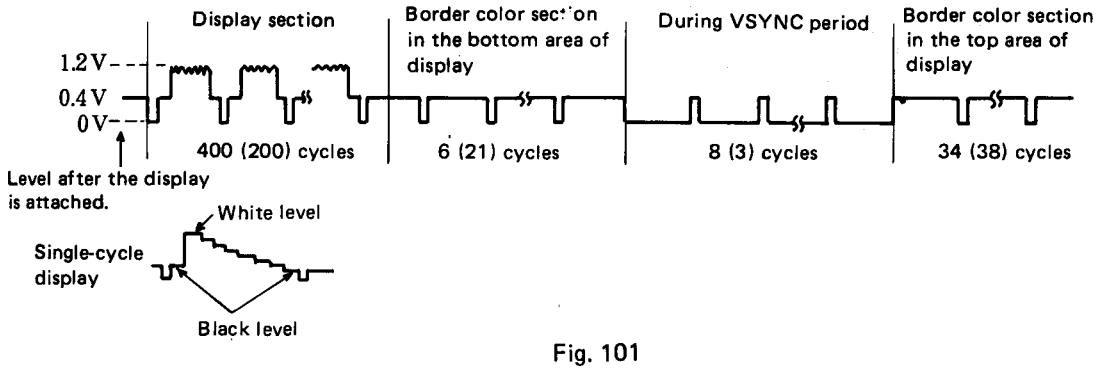


Fig. 101

For a monochrome display, gradation depends on the combined level of the $\overline{\text{R}}$, $\overline{\text{G}}$, and $\overline{\text{B}}$ inputs: That is, a white level is obtained when a full level of $\overline{\text{R}}$, $\overline{\text{G}}$, and $\overline{\text{B}}$ signals is applied, and a black level is obtained when the three signal levels are reduced to zero.

14-4 Timing charts

VDC2 timing

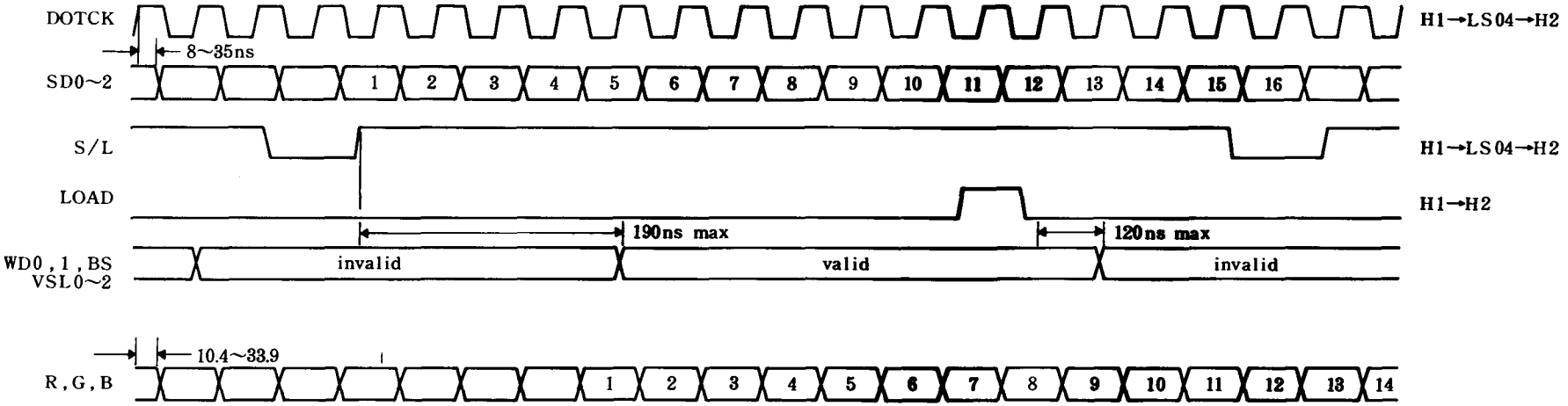


Fig. 102

VDC1, VDC2 internal register write timing

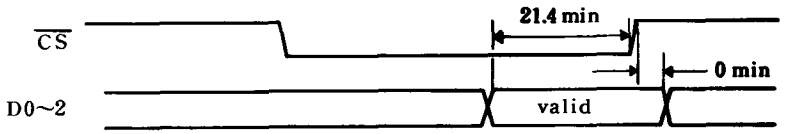


Fig. 103

VDC1 timing for display cycle (1)

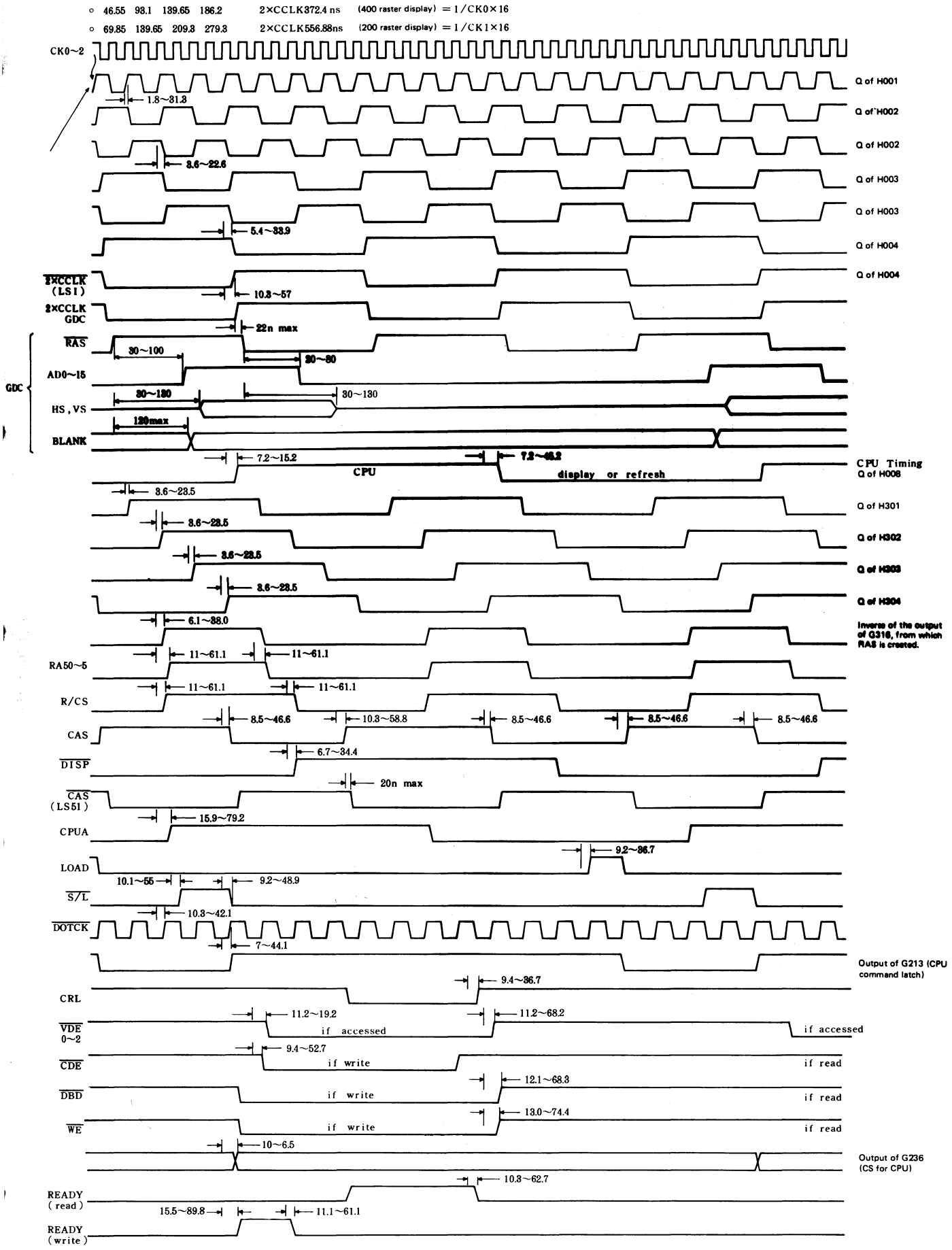
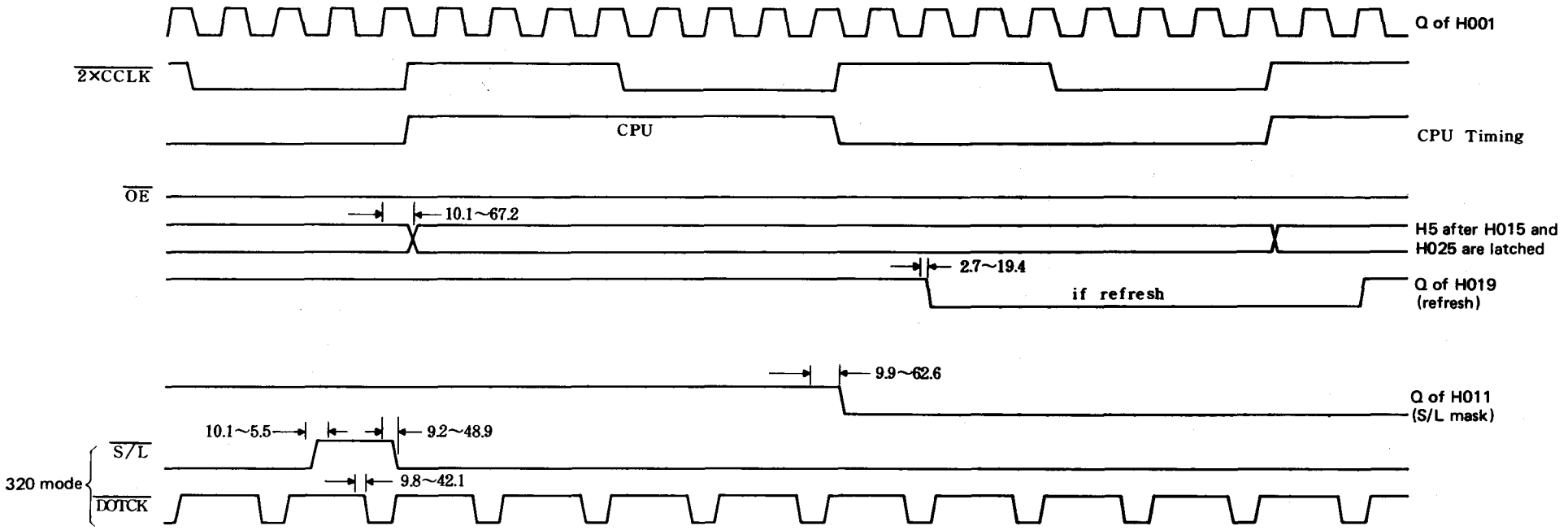


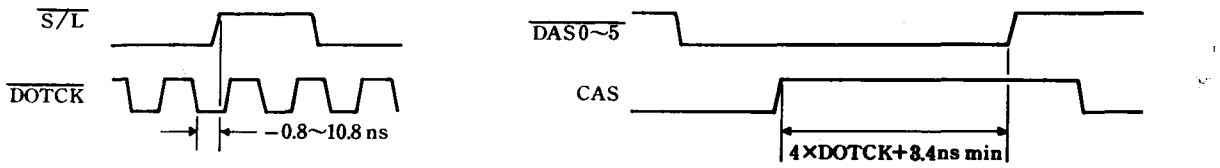
Fig. 104

VDC1 timing for display cycle (2)



The following timing relationships are given by forced arrangement.

Fig. 105



Figs. 106, 107

VDC1 timing for drawing cycle (1)

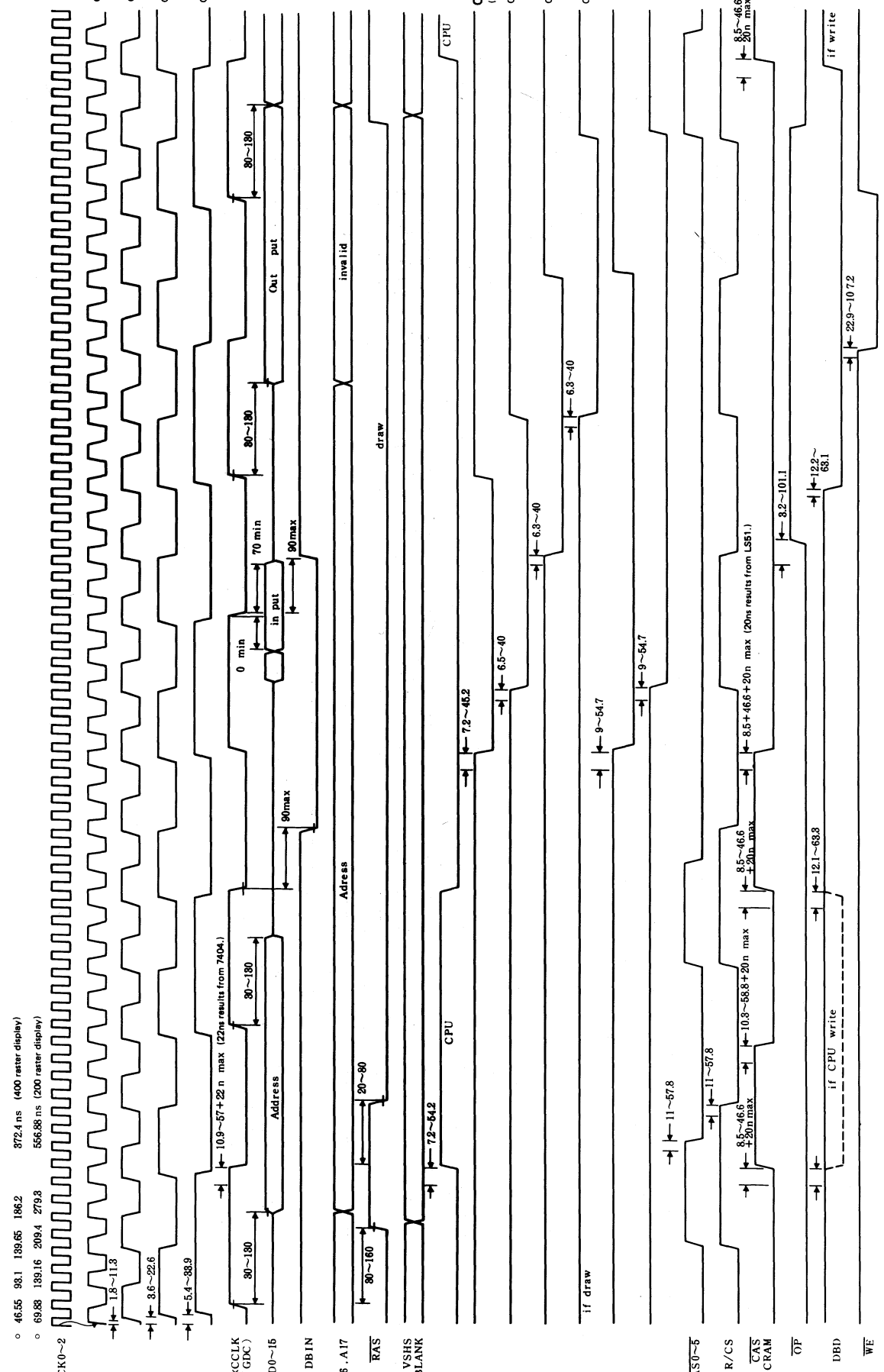


Fig. 108

VDC1 timing for drawing cycle (2)

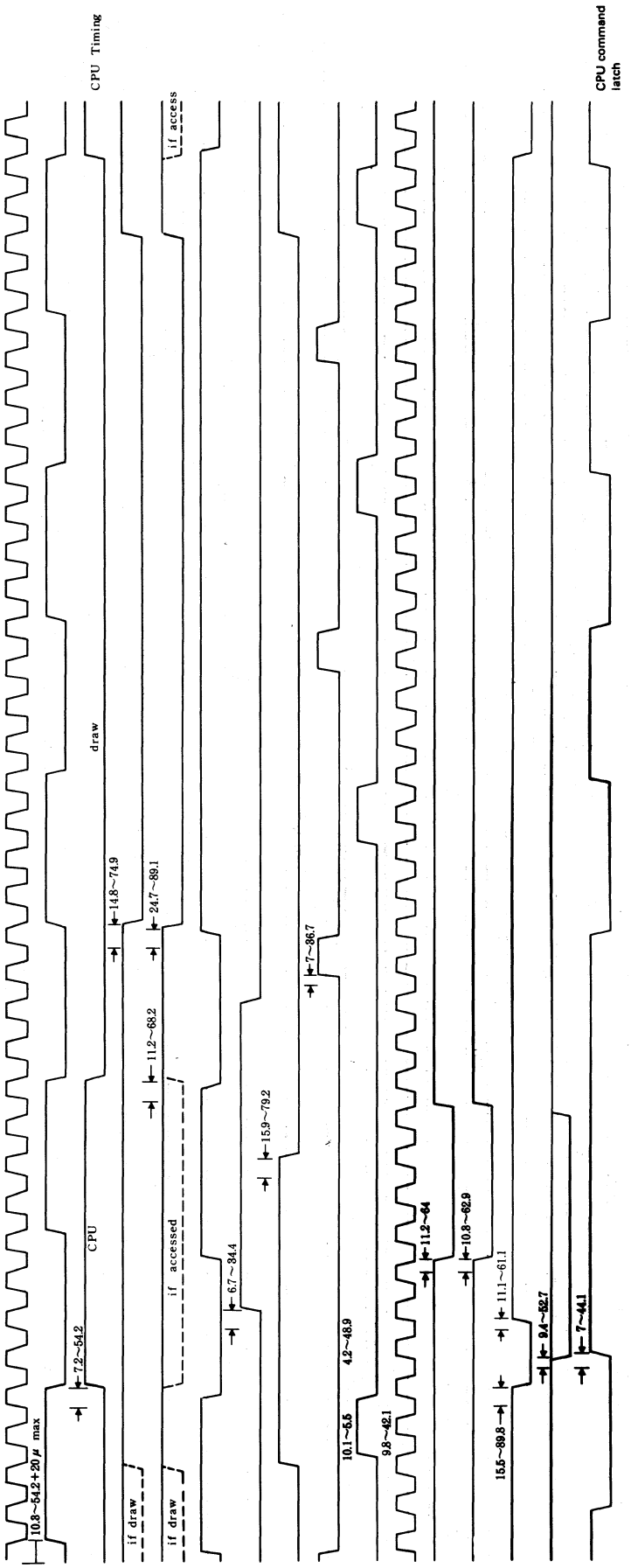


Fig. 109-a

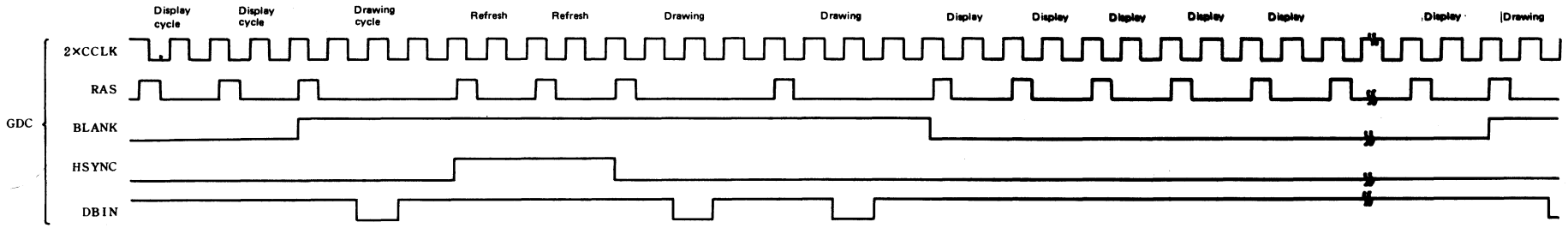


Fig. 109-b

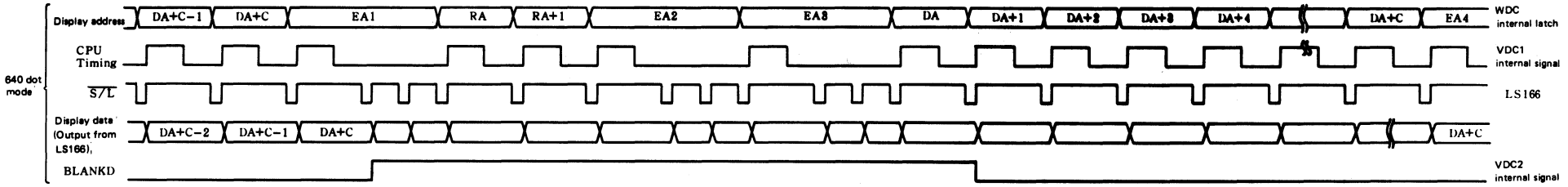
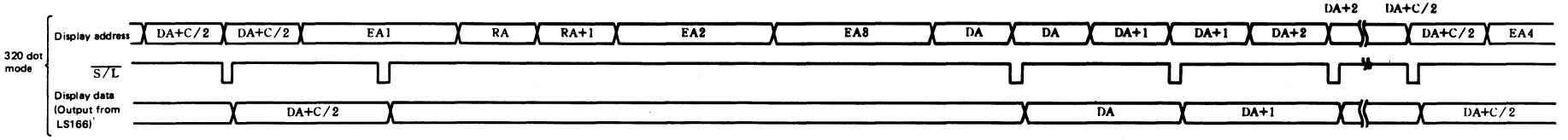


Fig. 109-c



DA : Display start address
C : C/R
EA : Drawing address
RA : Refresh address

Fig. 109-d

15. KEYBOARD AND KEYBOARD INTERFACE

15-1 Keyboard specifications

* Intelligent keyboard containing the 80C49 processor.
* 63 byte input buffer.
* Two key roll-over.
* Mode indicators for CAPS, and GRAPH.
* Two types of repeat functions can be specified by CPU commands.

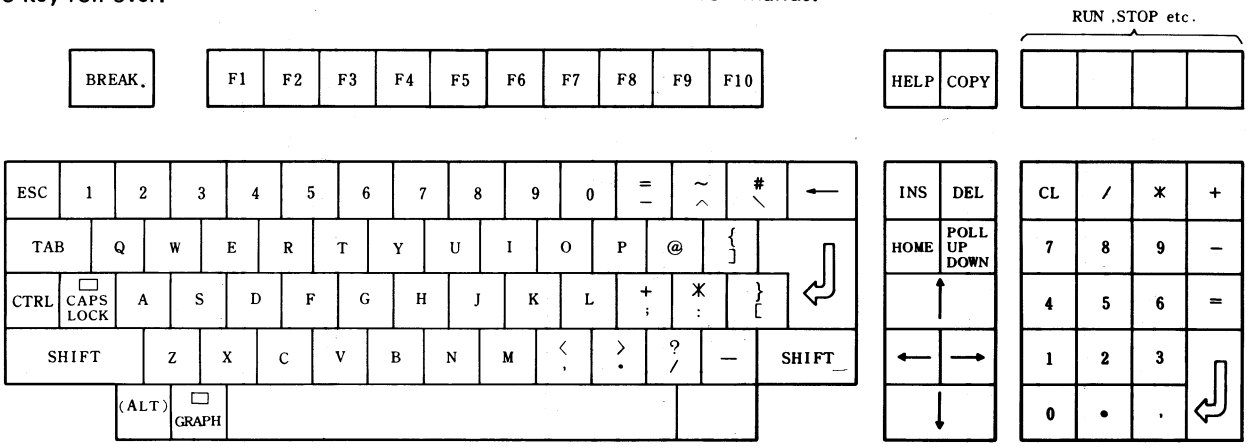


Fig. 110 (In the case of English type)

Special Keys

SHIFT: Used for uppercase shift or to provide the upper case shift functions (F11—F20) for the function keys (F1—F10).

CAPS: LOCK Used to fix shift character selection. If it is used with the Shift key, the shift and normal mode will be reversed.

GRAPH: Selects Graphic mode.

CTRL: Used to generate compressed commands.

ALT: Used to generate extended commands.

Keyboard mode

1) NORMAL mode: All keys on the keyboard are operative (to generate one byte data).

2) GRAPH mode: Selected with the GRAPH key to place the keyboard in the graphic mode (1 byte data).

Notes: * To clear the selected mode, operate the same mode select key or keys a second time.

* If the CTRL and ALT keys are depressed, the keyboard is placed in the normal mode (CAPS and SHIFT keys operative), with the exception that every piece of data consists of two bytes, with the first byte assigned to a CTRL ALG code, and the second byte assigned to the entry code.

Description of special keys

(A) SHIFT key

* Used to place the keyboard in the shift mode (used with other keys).
* Operation of the SHIFT key alone is invalid (no code is transferred to the CPU).

(B) CAPS key

* Used for shift character selection.
* Operative only in the normal mode.
* If used with the SHIFT key, shift and normal selection will be reversed.
* If the CAPS key alone is used, no operation will result (no code is transferred to the CPU).

(C) GRAPH key

* **Used to place the keyboard in the Graphic mode. When operated, the pertinent code is transferred to the CPU (operation of the GRAPH key alone is valid).**
* **All other keys produce the codes the same as those in the normal mode.**

(D) CTRL key

* **When this key is operated, entry data consists of two bytes: a normal-mode key code followed by a CTRL code. Operation of the mode keys (GRAPH) are ignored. After the CTRL key is operated, the CAPS and SHIFT keys remain valid.**
* **Operation of the CTRL key alone is not valid (no code is assigned).**

(E) ALT key

* **After the ALT key is operated, entry data consists of two bytes (same as for CTRL).**
* **Used to generate extended command codes.**
* **Effective when used with other keys.**
* **The pertinent code is transferred to the CPU when operated.**

15-2 Keyboard interface

(1) Block diagram

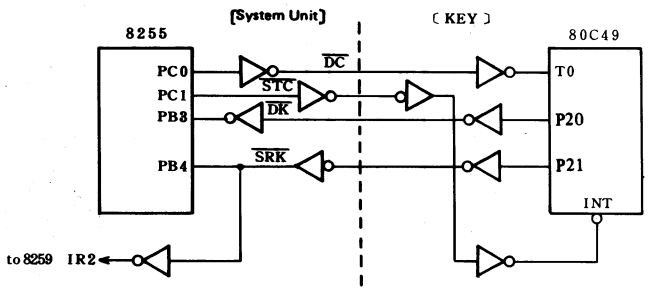


Fig. 111

Table 43

Direction / Signal name	CPU to keyboard	Keyboard to CPU
$\overline{DC}$	Send data	'READY' signal
$\overline{STC}$	Strobe	Request to Send (strobe for key data)
$\overline{DK}$	READY and ACK signals	Send data
$\overline{SRK}$	None	Request to Receive (CPU)

(2) Key data transfer procedure

1) From keyboard to CPU

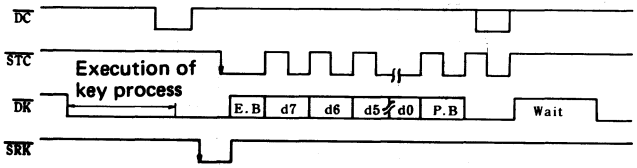


Fig. 113

To disable both the keyboard and the CPU interrupt, set both $\overline{DC}$ and $\overline{DK}$ to zero.

Keyboard: When key search, code translation, and other necessary entry data processing is completed, the keyboard starts transferring entry data to the CPU. First, it waits until $\overline{DC}$ is set to one. The waiting time is normally 3ms; for direct keys, it is 1ms. If a time-out occurred, the keyboard exits the data send sequence. When $\overline{DC}$ is set to one, the keyboard sets $\overline{SRK}$ to zero to interrupt the CPU.

CPU: After acknowledging the interrupt, the CPU verifies that $\overline{DK}$ is zero. If $\overline{DK}$ is one, the CPU identifies the transferred data as noise, and exits the interrupt service routine. It then sets $\overline{STC}$ to zero.

Keyboard: When $\overline{STC}$ is set to one, the keyboard waits until $\overline{STC}$ is set to zero. The maximum waiting time is 500ms. If a time-out occurred, keyboard control returns to the initialization routine. When verifying $\overline{STC}$=0, the keyboard send data EB and $\overline{SRK}$ to one.

CPU: Receiving the EB, the CPU sets STC to 1 to request the keyboard for the next data send.

Keyboard: Seeing $\overline{STC}$ is set to one, the keyboard waits for $\overline{STC}$ to be set to zero.

CPU: Sets $\overline{STC}$ to zero to read data from the keyboard, then sets $\overline{STC}$ again to one to request the keyboard for the next data send.

Keyboard: When $\overline{STC}$ is set to one, the keyboard sets P.B. and waits for $\overline{STC}$ to be reset to zero. When $\overline{STC}$ is set again to one, it sets DK to zero.

CPU: Sets $\overline{STC}$ to zero to read P.B. then sets $\overline{STC}$ to one to set the result of the parity check into $\overline{DC}$. If a parity error occurred, $\overline{DC}$ is zero; if no parity error occurred, $\overline{DC}$ is 1. The CPU sets $\overline{STC}$ to one to complete the transfer sequence.

Keyboard: When $\overline{STC}$ is set to zero, the keyboard reads the result of the parity check. When $\overline{STC}$ is set to one, it sets $\overline{DK}$ to one to enable an interrupt from the CPU, and completes the data transfer sequence. If a parity error was detected, the keyboard terminates the data transfer sequence, then tries the same data send again.

* Repeat nine times.

2) Form CPU to keyboard

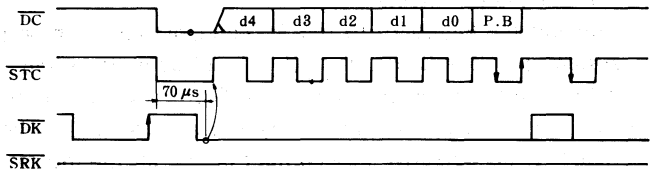


Fig. 114

CPU: Waits for up to 100ms for $\overline{DK}$ to be set to one. If $\overline{DK}$ is still zero 100ms later, the CPU identifies it as a keyboard error and exits the sequence. After verifying that $\overline{DK}$ is one, the CPU sets $\overline{DC}$ and $\overline{STC}$ to zero, to interrupt the keyboard.

Keyboard: When the keyboard is interrupted by the CPU, it enters the data receive sequence and verifies $\overline{DC}$=0. If $\overline{DC}$ is one, the keyboard identifies $\overline{STC}$=0 as noise, and exits the interrupt sequence. If $\overline{DC}$ is zero, it sets $\overline{DK}$ to zero.

CPU: Verifies that $\overline{DK}$ is zero 70μs after interrupting the keyboard. The CPU then sets STC to one to set d4, then resets $\overline{STC}$ to zero again.

Keyboard: Seeing $\overline{STC}$ is set to one, the keyboard reads data when $\overline{STC}$ is reset to zero.

CPU: Sets $\overline{STC}$ to one to set data, then resets $\overline{STC}$ to zero.

Keyboard: Reads P.B. to check parity, then sets the result of this parity check when $\overline{STC}$ is set to 1. If no parity error occurred, it sets $\overline{DK}$ to one; if a parity error occurred, $\overline{DK}$ is zero. The keyboard sets $\overline{DK}$ to zero when $\overline{STC}$ is reset to zero.

CPU: Sets $\overline{STC}$ to one to read the result of the parity check. It then temporarily sets $\overline{STC}$ to zero and then sets it again to one, to terminate operations.

* Repeat five times.

(3) Keyboard check method

(A) If the keyboard is locked up:

Checking the keyboard processor

Connect the keyboard to the System Unit, then turn on the system without operating any keys. If only the CAPS indicator comes on, ROM check for the keyboard processor (80C49) is normal. If all the indicators come on, it indicates a ROM check error occurred. Probably the keyboard processor (80C49) is malfunctioning.

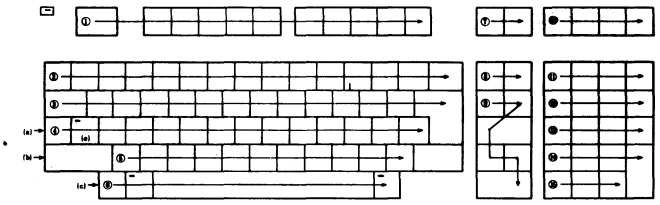


Fig. 115

(B) Some keys are inoperative:

Checking key contacts

Connect the keyboard to the System Unit, and turn on the system with the CTRL and ALG (a, c) keys depressed and held. After making sure all the indicators come on, press the keys in the order shown by the arrows in the above figure. If no defective key contact exists, all the indicators will go off. If any defective contact exists, all the indicators will remain on. If a wrong key is pressed and the indicators come on, they will go off when the correct key is subsequently pressed.

If no contact trouble exists when all the keys have been operated, the CAPS indicator will come on, indicating that the key check was normal.

15-3 Key search timing

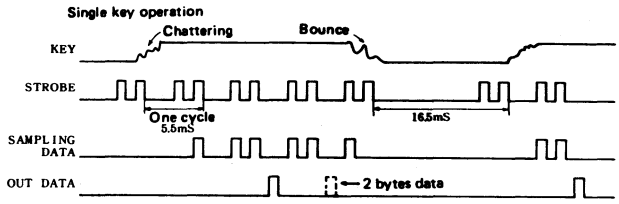


Fig. 116

To prevent chattering and bounce, the same key data is checked twice during each search, and only matching key data is regarded as correct. While the search cycle is 5.5ms, it is extended to 16.5ms if a bounce occurs.

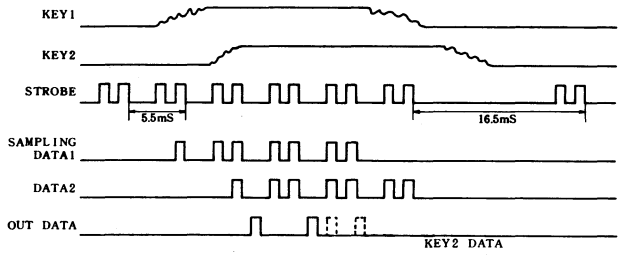


Fig. 117

Key search sequence for two-key operation is the same as that for single key operation. When two keys are simultaneously pressed, key data for the first and second keys are successively transferred.

15-4 Eight-bit keyboard processor μPD80C49

Highlights

1) Single-chip, 8-bit microprocessor.
2) Built-in 2K x 8 bit ROM.
3) On-chip 128K x 8 bit RAM.
4) Interruption service capability.
5) I/O port: 8 bits x 2
   Data bus (serving also as I/O port): 8 bits x 1
6) Built-in clock generator.
7) Single +2.5 to +6V power supply.

Pin configuration

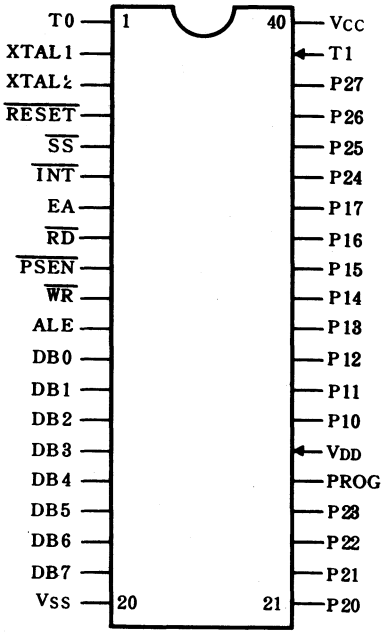


Fig. 118

Pin functions

P10-P17:	I/O port (port 1)
P20-P27:	I/O port (port 2)
DB0-DB7:	Data bus
T0, T1:	Test
$\overline{INT}$:	Interrupt
$\overline{RD}$:	Read
$\overline{WR}$:	Write
ALE.	Address latch enable
$\overline{PSEN}$:	Program store enable
$\overline{RESET}$:	Reset
$\overline{SS}$:	Single step
EA:	External access
XTAL1, 2:	Quartz inputs
VDD:	Standby control

Keyboard processor (80C49) signal functions

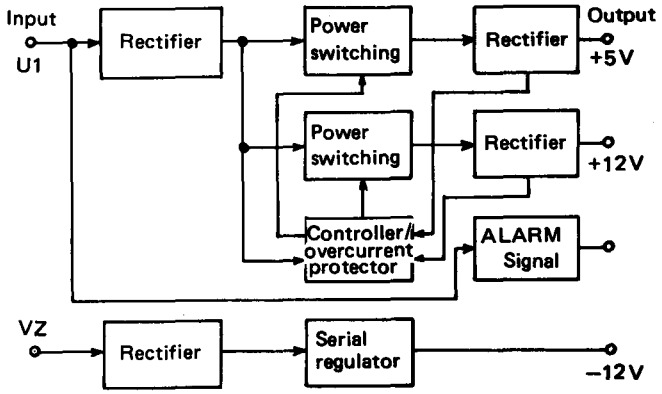
Table 44

Pin No.	Signal name	IN/OUT	Description
1	T0	IN	Data or $\overline{\text{READY}}$ signal input from the System Unit
2	XTAL1	IN	Accepts a quartz signal (6MHz) for the internal clock oscillator.
3	XTAL2	IN	Accepts a quartz signal (6MHz) for the internal clock oscillator.
4	RESET	IN	Initialization input of 80C49
5	SS	IN	+5V
6	$\overline{\text{INT}}$	IN	CPU interrupt strobe input ($\overline{\text{STC}}$)
7	EA	IN	GND
8	$\overline{\text{RD}}$	–	N.C
9	$\overline{\text{PSEN}}$	–	N.C
10	$\overline{\text{WR}}$	–	N.C
11	ALE	–	N.C
12 19	DB0 DB7	IN	Returns signals from the keyboard.
20	Vss	IN	GND
21	P20	OUT	Send data to the System Unit ($\overline{\text{DK}}$)
22	P21	OUT	Data enable/start signal ($\overline{\text{SRK}}$) to CPU
23	P22	OUT	Enables data send to the mouse (CTS)
24	P23	–	N.C
25	PROG	–	N.C
26	VDD	IN	+5V
27 30	P10 P13	OUT	Strobe to the keyboard.
31	P14	OUT	CAPS indicator drive signal
32	P15	OUT	GRAPH indicator drive signal
33	P16	OUT	N.C
34	P17	–	N.C
35	P24	–	N.C
36	P25	–	N.C
37	P26	–	N.C
38	P27	–	N.C
39	T1	IN	Mouse data input (TXD)
40	Vcc	IN	+5V power supply

16. POWER CIRUCIT

16-1. Circuit Configuration

(1) Block diagram



(2) The above figure, an AC input of 50/60 Hz is rectified into a DC current which is then converted into an alternate current of 50 kHz to produce +5 V and +12 V output voltages. For the control of the output voltage, the output voltage is detected and controlled of its pulse width to drive the transistor in the power switching section. As for −12 V, and AC input of 50/60 Hz is rectified into a DC current of which voltage output is stabilized by the serial regulator.

16-2. Description of the Power Supply Circuits

(1) Rectifier circuit

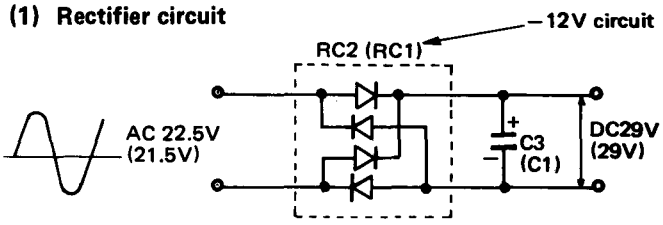


Fig. 1 Rectifier circuit

Figure 1 shows the rectifier circuit. Input of AC local voltage for the power transformer is converted into the secondary output voltage of 22.5 V AC and rectified to obtain 29 V DC from which deriverd +5 V and +12 V outputs. Enclosure by dotted line in Fig. 1 shows the −12 V rectifier circuit.

(2) +5V power switching

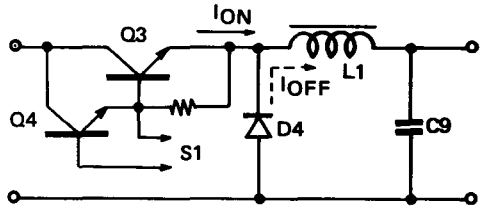


Fig. 2 Power switching

In Fig. 2, S1 is connected to the base of Q4 and the current ION flows through when Q3 becomes active. When Q3 turns inactive, the current IOFF flows through. So, by controlling the on/off time ratio, it produces a stable voltage supply.

Fig. 3 shows the Q3 driving circuit.

1) When Q5 turns active, the current ION flows through in the direction shown with the solid line and makes Q3 and Q4 active.
2) When Q5 turns inactive, the current IOFF flows through in the direction shown with the broken line and makes Q3 and Q4 reverse biased so as to delay speed of Q3 at the falling edge.

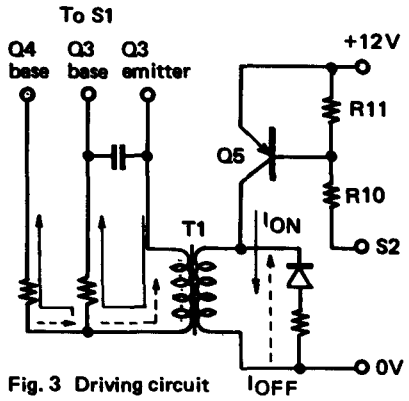


Fig. 3 Driving circuit

(3) +12V power switching

This driving circuit performs the same as the +5V power switching action by means of Q6.

Q7 is driven by M1 (8 and 11 pins). (Fig. 4)

(4) −12V output control

In this circuit the unstable voltage supply from the power transformer is obtained the stable supply of −12V via the dropper. If the output is lower than the reference voltage, it makes the Q1 base current increased so as to rise the output voltage. If it is higher, the base current is supplied to D1 to increase the Q1 resistance so as to restrict the output voltage. In this manner, the output voltage supply is maintained to a stable level. (Fig. 5)

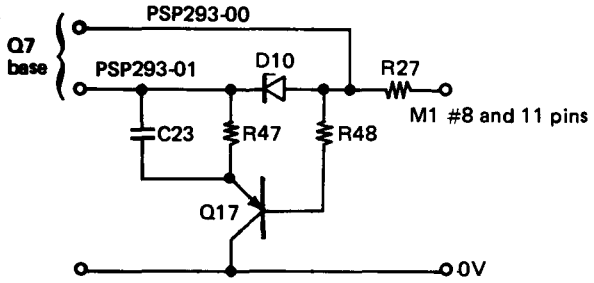


Fig. 4 Drive circuit

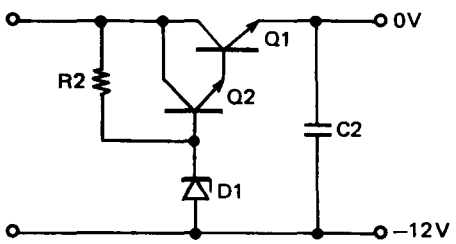


Fig. 5 −12V output control circuit

(5) Overcurrent protect circuits

- +5V overcurrent protect circuit

The voltage proportionate to the output current is created in R24. When it becomes equal to the voltage difference with R15 and VR4, it starts to restrict the current. As this causes the output voltage to drop, it also reduces the R15 and VR4 voltage. (Fig. 6)

- +12V overcurrent protect circuit

The voltage proportionate to the output current is created in R36. When it becomes equal to the voltage difference with VBE of Q11 (R37 voltage), it starts to restrict the current. As this causes the output voltage to drop, it also reduces the R37 voltage. (Fig. 7)

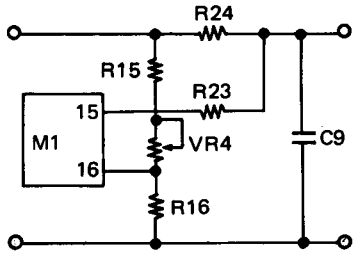


Fig. 6 +5V overcurrent protect circuit

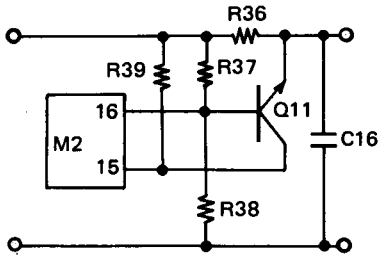


Fig. 7 +12V overcurrent protect circuit

(6) ALARM signal

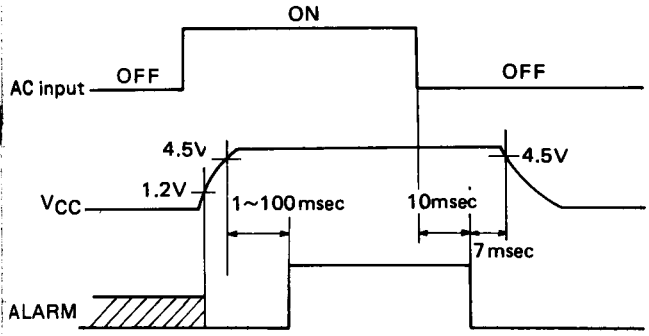


Fig. 8 ALARM signal sequence

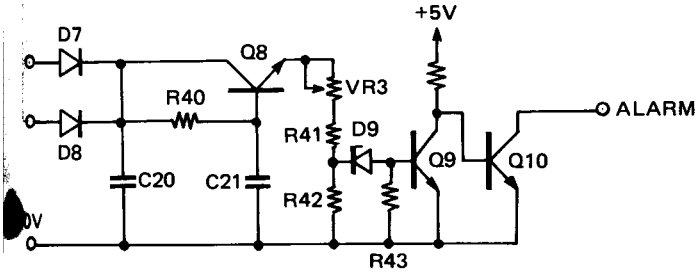


Fig. 9 ALARM signal circuit

The signal ALARM is a signal that has a sequence shown in Fig. 7. The input voltage is detected by the voltage which the power transformer secondary side is rectified, to create the signal ALARM. (Figs. 8 and 9) The rising edge is delayed at power on by the network composed of R40 and C21, and it is determined by the discharge of C21, R41, R42, and VR3 at power off.

(7) Adjustments

VR1	+5V voltage adjustment: 5V ± 0.02V
VR2	+12V voltage adjustment: +12V ± 0.05V
VR4	+5V output current adjustment: 9.2 A ± 0.2 A
VR3	ALARM adjustment: 5ms faster than 5V falling edge

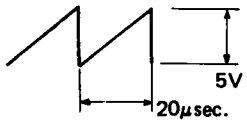
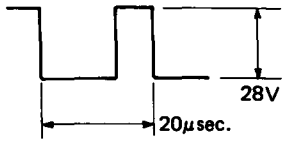
16-3 Troubleshootings

(1) Hints and tips

Check the following points to achieve faster trancing of trouble cause.

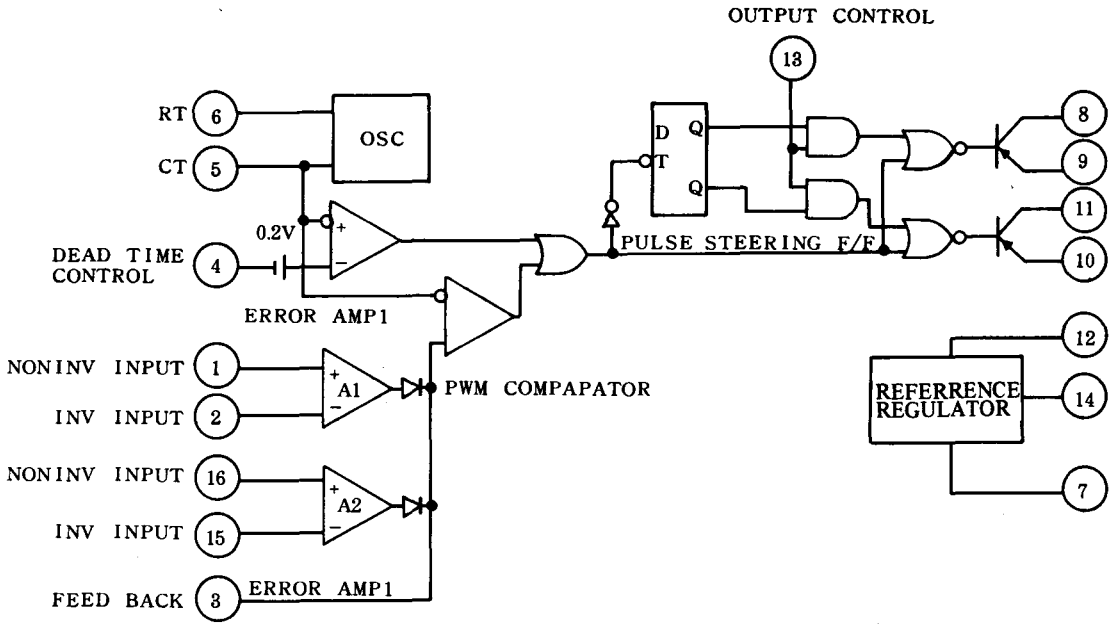
1) Do not try to remove the printed board at first. Visually check open wire, contact failure, and improperly soldered wire, or burnt resistor, etc.
2) Unfasten the power input connector (V1, V2: CN5) and check for any failure such as a failure in the primary side of the power transformer.
3) Observe the following causing in removing the printed board.
   - Screw tightening torque
     - Tightening torque for the screw used to secure electronic component with the chassis: 4 kgfcm
     - Tightening torque for other screws: 6 kgfcm
   - Take care not to open the jumper (JP-1) that used between printed board.
   - Handle the insulation sheet with care.
4) Have the following tools ready.
   - Oscilloscope
   - 200 VAC power supply regulator (SLIDAC)
   - Voltmeter (1–50 VAC/VDC)
   - Ammeter (0.1–15 amperes AC/DC)
   - Dummy load (or CPU unit)
   - Power supply transformer

(2) Checking the trouble cause

Check procedure	Trouble phenomenon	Defective location
(START) 1-1. Check the +12V output.	Check that; +12V output load is 0.5A. +5V is free load. −12V is free load.	
1-2. Connect the oscilloscope to M2 −5 pin.	Set the oscilloscope to 1V/div, 5μs/div.	
2-1. Slowly increase the input voltage.	Turn input OFF if the input current should exceed 1A when it is increased to 10V.	RC1, RC2, Q3, Q4, Q6, Q7, D4, D7, D8, C3, C20. (Q12) applies to 01.
3-1. Check if a triangle waveform is observed. If no, replace the parts. Otherwise, go to 4-1.	Make sure that it is as shown below.  	M1, M2, C5, C25, F1
4-1. While observing the waveform between Q6 and VCE, increase the input voltage.	Connect oscilloscope probes to Q6 and VCE and make sure that the waveform appears as shown below.  	Q5, Q6, Q7, M1, M2, D6. (Q12, D10) applies to 01.
5-1. Confirm appearance of +12V output voltage.	Adjust the +12V output voltage by means of VR2. Clockwise turn of the VR2 increases the voltage. Short current of +12V is 1A.	M2, Q11, VR2, R36, (Q12, D10) applies to 01.
6-1. Check +5V output.	Check that: +5V output has a load of 0.2A. +12V output is free load. −12V output is free load.	
6-2. Increase input voltage by observing the waveform between Q3 and VCE. Check if oscillating. If no, replace the parts. If yes, go to 7.	Connect the oscilloscope and observe the waveform between Q3 and VCE. (See Item 4.) Adjust the input voltage to 22V.	M1, Q4, Q5, D4, D5, C9, C10.

Check procedure	Trouble phenomenon	Defective location
7-1. Check +5V output voltage.	To adjust +5V, use the VR1, Clockwise turn of VR1 increases the voltage. Short current of +5V is 1 to 2A.	M1, VR1, C9, C10
8-1. Check −12V output.	Check that: +5V output has a load of 0.2A. −12V output has a load of 0.05A. +12V output is free load.	
8-2. While observing the −12V output voltage, increase the input voltage. Check if −12V output voltage produced. If no, replace the parts. If yes, go to next. Check the −12V output voltage.	If the output voltage of −12V ±15% is not seen after raising the input voltage slowly to 16 VAC.	RC1, Q1, Q2, D1, R1
9-1. Check ALARM.	Connect the +5V line to the ALARM pin in a manner shown below. +5V 1KΩ Then, there should appear +5V between 0V and ALARM pins.	Q8, Q9, Q10, D7, D8, D9, C20, C21, VR3
9-2. Increase the input voltage. Check if ALARM is +5V. If no, replace the parts. If yes, to go END. END	When the input voltage is slowly increased to 18 VAC, the voltage on this pin changes from 0V to +5V (at an input of 15VAC). It needs to adjust VR5 to attain proper adjustment of the input voltage, when three is a problem.	• Do not try to manipulate VR5. • Use the memory oscilloscope when a time setup is used. • Clockwise turn of VR3 makes a time difference shorter between AC input off a ALARM.

Internal circuit of IC(MB3759)



17. SELF CHECK

17-1 Self check functions

According to the system switch setting, the MZ-5500 automatically provides the following self check items using the check programs contained in the ROM:

Table 45

- RAM check (system RAM)
- ROM check (IPL ROM)
- MFD (mini-floppy disk drives)

The details of the check items are:

1) RAM capacity check.
2) Data bus check
3) Address bus check
4) Read/write check on entire memory locations
5) Refresh signal check
6) Refresh check
7) ROM check
8) MFD read/write check

If an error is detected through the self check, the operator is asked by an audible sound alarm and error message on the video monitor.

During self check execution, each check stage is identified by a short "beep," which should not be taken as an error alarm.

17-2 Check procedures

Self checking may be done as follows:

(1) Set section 2 of the system DIP switch (located on the bottom of the System Unit) to ON, with the System Unit left turned off.

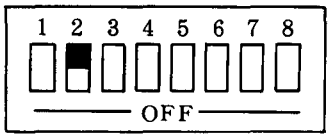


Fig. 1 System DIP switch

(2) Turn the system on. The check program will automatically start running, and the total RAM capacity will appear first on the screen (see Fig. 2).

```
256KB
```

Fig. 2 RAM capacity display

(3) Each time a check result is identified to be normal, it is indicated by a short "beep." For example, the following message will appear if the RAM check was passed:

```
RAM-OK
```

Fig. 3 Message for normal RAM check result

(4) If an error occurred, it is alerted by a long "beep." The long "beep" will sound once for a RAM check error, twice for a ROM check error, and three times for an MFD check error. The pertinent error type will be shown on the display as shown in Fig. 4. The details of each error type will be described later. Once the error message appears on the screen, check execution pauses for five seconds, then the screen is cleared and check execution proceeds with the next step.

```
    *       *
FEDCBA9876543210
40000H
ERROR 05
```

Fig. 4 Error message example

(5) When the RAM and ROM check is completed, a message as shown in Fig. 5 will appear. Insert the checking diskette (refer to the note below) into the drive to be checked. Press the RESET switch on the front of the System Unit to start the drive check. When the drive check is completed, the message shown in Fig. 5 will appear again. If you wish to check another drive, remove the checking disk from the first drive and insert it into the second drive, then press the RESET switch.

```
EXCHANGE DISK
PUSH RESET BUTTON
```

Fig. 5 MFD check prompt message

(6) When all check items are completed, turn off the system, and set section 2 of the system DIP switch back to the OFF position.

Note: For the checking diskette, use a formatted blank diskette with no write protect label attached.

17-3 Self test messages on display

17-3-1 Normal message display

Table 46

Message	Meaning
RAM-OK	The RAM check was okay.
ROM-OK	The ROM check was okay.
EXCHANGE DISK PUSH RESET BUTTON	Replace the diskette with the checking diskette and press the RESET switch.
MFD-OK	The MFD test was passed.

17-3-2 Error message display

Table 47

Message	Meaning	"Beep" count
ERROR 00	Stack area cannot be reserved (Note 1)	10
ERROR 01	Data bus error (Note 2)	1
ERROR 02	$\overline{BHE}$ or A0 error.	1
ERROR 03	Hardware error such as address line short circuit (Note 3).	1
ERROR 04	Hardware error such as discontinuity of address line, or a short circuit to the supply or other signal line (Note 3).	1
ERROR 05	RAM error (read/write error) (Note 4).	1
ERROR 06	DMAC error.	1
ERROR 07	Written data was lost.	1
ERROR 08	High order ROM error.	2
ERROR 09	Low order ROM error.	2
ERROR 10	MFD reads or writes wrong data.	3
ERROR 11	MFD protect error.	3
ERROR 12	MFD read/write error.	3
ERROR 13	Hardware error.	3

17-3-3 Other error messages

Table 48

Message	Meaning
* * FEDCBA9876543210	*Numeral identified by an asterisk (*) is not correct (A16 is represented by 0).
30000H	Error address on memory.

17-3-4 RAM capacity message

Table 49

Message	Meaning
128KB (128KB, 256KB, or 512KB)	Presently existing RAM capacity (if the displayed value does not agree with the actual capacity, the RAM is defective or an error exists on address lines A18 or A19.

Note 1. If this message appears, check execution will be aborted.

Note 2. Also displays the data bus on which the error occurred (see Fig. 6).

Note 3. Also displays the address line on which the error occurred (A16—A1) (see Fig. 7).

Note 4. Displays the error bit (F-0), along with the address (00000H—70000H) (see fig. 4).

```
  *     *
FEDCBA9876543210 ←—— (D15～D0)
ERROR 01
```

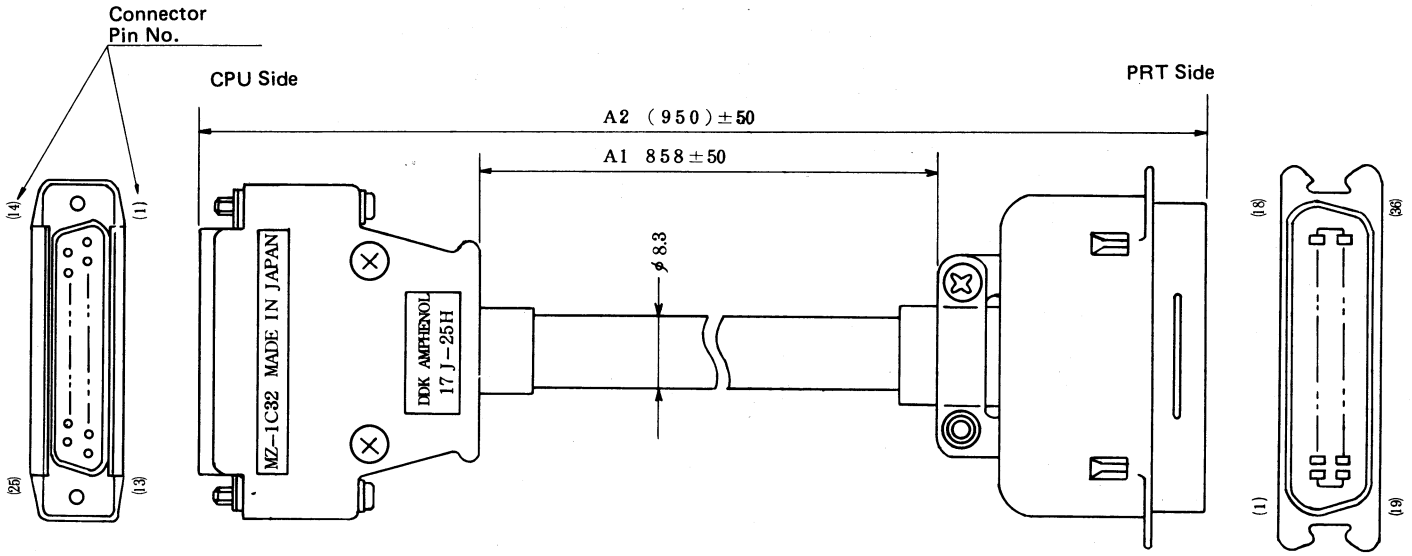
Fig. 6 Error 01 Message

```
  *  *
FEDCBA9876543210 ←—— (A16～A1)
ERROR 03
      ↖ Or 04
```

Fig. 7 Error 03 or 04 Message

18. TERMINAL VIEW OF CABLE

MZ-1C32
Printer Cable

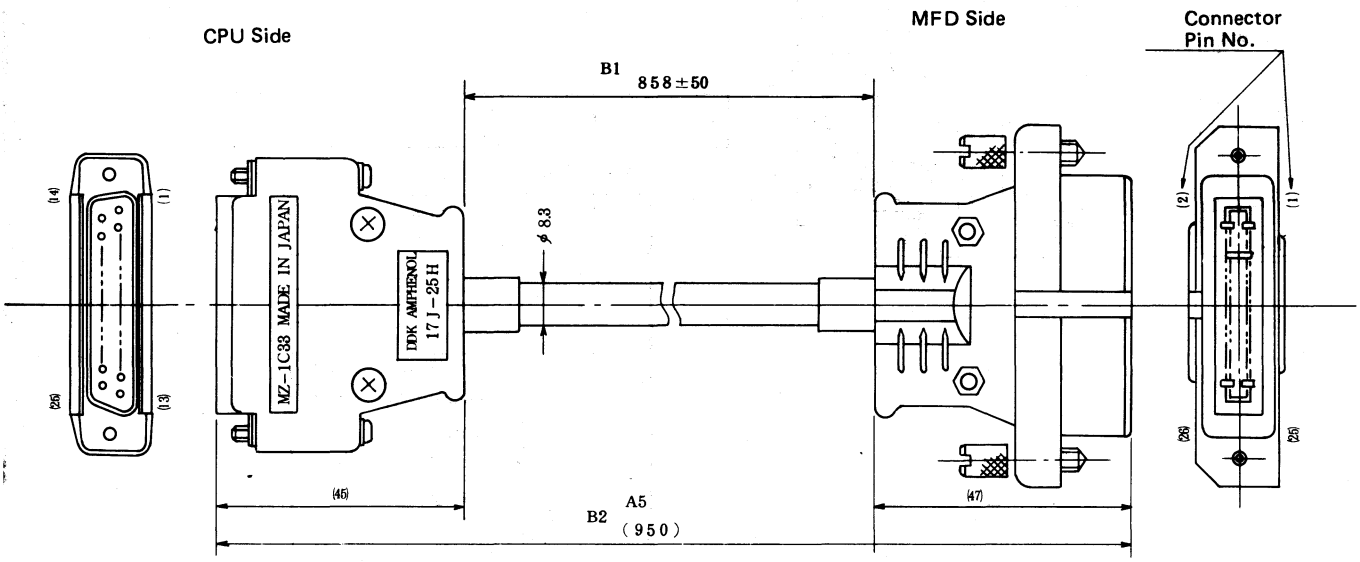


CPU side Pin No.	Signal name	Wire color	PRT side Pin No.	CPU side Pin No.	Signal name	Wire color	PRT side Pin No.
1	$\overline{\text{STROBE}}$	Orange/Red (A)	1	14	GND	Orange/Black (A)	19
2	DATA1	Gray/Red (A)	2	15	GND	Gray/Black (A)	20
3	DATA2	White/Red (A)	3	16	GND	White/Black (A)	21
4	DATA3	Yellow/Red (A)	4	17	GND	Yellow/Black (A)	22
5	DATA4	Pink/Red (A)	5	18	GND	Pink/Black (A)	23
6	DATA5	Orange/Red (B)	6	19	GND	Orange/Black (B)	24
7	DATA6	Gray/Red (B)	7	20	GND	Gray/Black (B)	25
8	DATA7	White/Red (B)	8	21	GND	White/Black (B)	26
9	DATA8	Yellow/Red (B)	9	22	GND	Yellow/Black (B)	27
10	$\overline{\text{ACK}}$	Pink/Red (B)	10	23	GND	Pink/Black (B)	28
11	BUSY	Orange/Red (C)	11	24	$\overline{\text{SRES}}$	Orange/Black (C)	31
12	PE	Gray/Red (C)	12	25	SELECT	Gray/Black (C)	13
13	–						

This hole is sometimes blocked
off at the Computer 25-way socket.

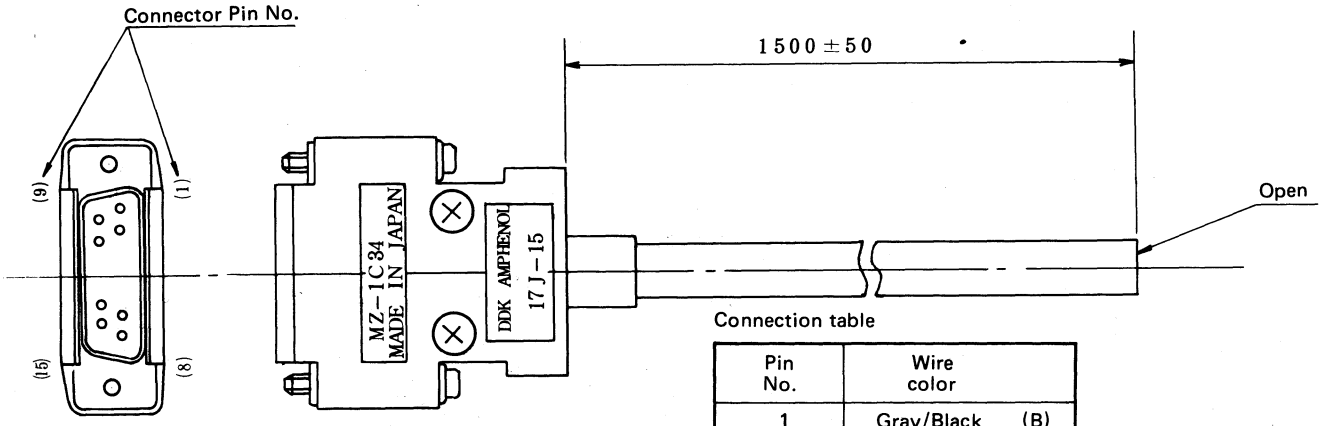
If it is, remove PIN 13 from the
25-way plug at the Computer end
of the Printer lead (in any case,
there is no connection on this pin)

MZ-1C33
MZ-5500 MZ-1F02 Expantion MFD



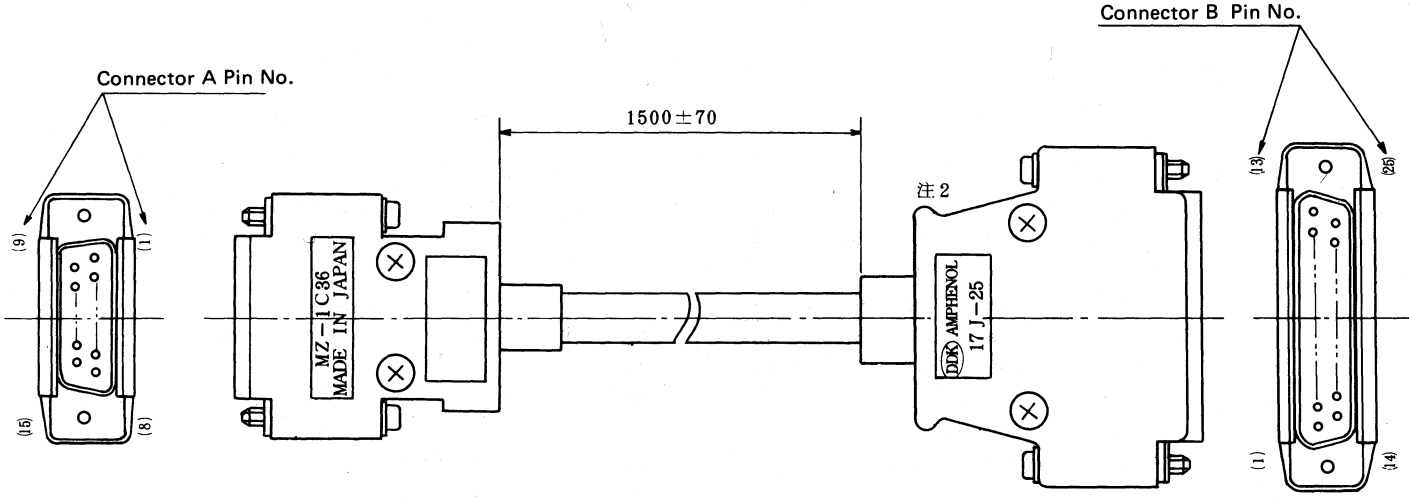
CPU side Pin No.	Signal name	Wire color	MFD side Pin No.	CPU side Pin No.	Signal name	Wire color	MFD side Pin No.
1	$\overline{\text{INDEX}}$	Gray/Red (A)	3	14	$\overline{\text{SEL0}}$	Pink/Red (A)	9
2	$\overline{\text{SEL2}}$	White/Red (A)	5	15	$\overline{\text{SEL1}}$	Orange/Red (A)	1
3	$\overline{\text{SEL3}}$	Yellow/Red (A)	7	16	GND	Pink/Black (A)	6
4	$\overline{\text{MOTOR ON}}$	Orange/Red (B)	11	17	GND	Orange/Black (B)	8
5	$\overline{\text{DIRECTION}}$	Gray/Red (B)	13	18	GND	Gray/Black (B)	10
6	$\overline{\text{STEP}}$	White/Red (B)	15	19	GND	White/Black (B)	12
7	$\overline{\text{WR DATA}}$	Yellow/Red (B)	17	20	GND	Yellow/Black (B)	14
8	$\overline{\text{WR GATE}}$	Pink/Red (B)	19	21	GND	Pink/Black (B)	16
9	$\overline{\text{TRACK0}}$	Orange/Red (C)	21	22	GND	Orange/Black (C)	18
10	$\overline{\text{NR PR}}$	Gray/Red (C)	23	23	GND	Gray/Black (C)	20
11	$\overline{\text{RD DATA}}$	White/Red (C)	25	24	GND	White/Black (C)	22
12	$\overline{\text{SIDE}}$	Gray/Black (A)	26	25			
13	$\overline{\text{READY}}$	Orange/Black (A)	24				

MZ-1C34
RS-232C Cable



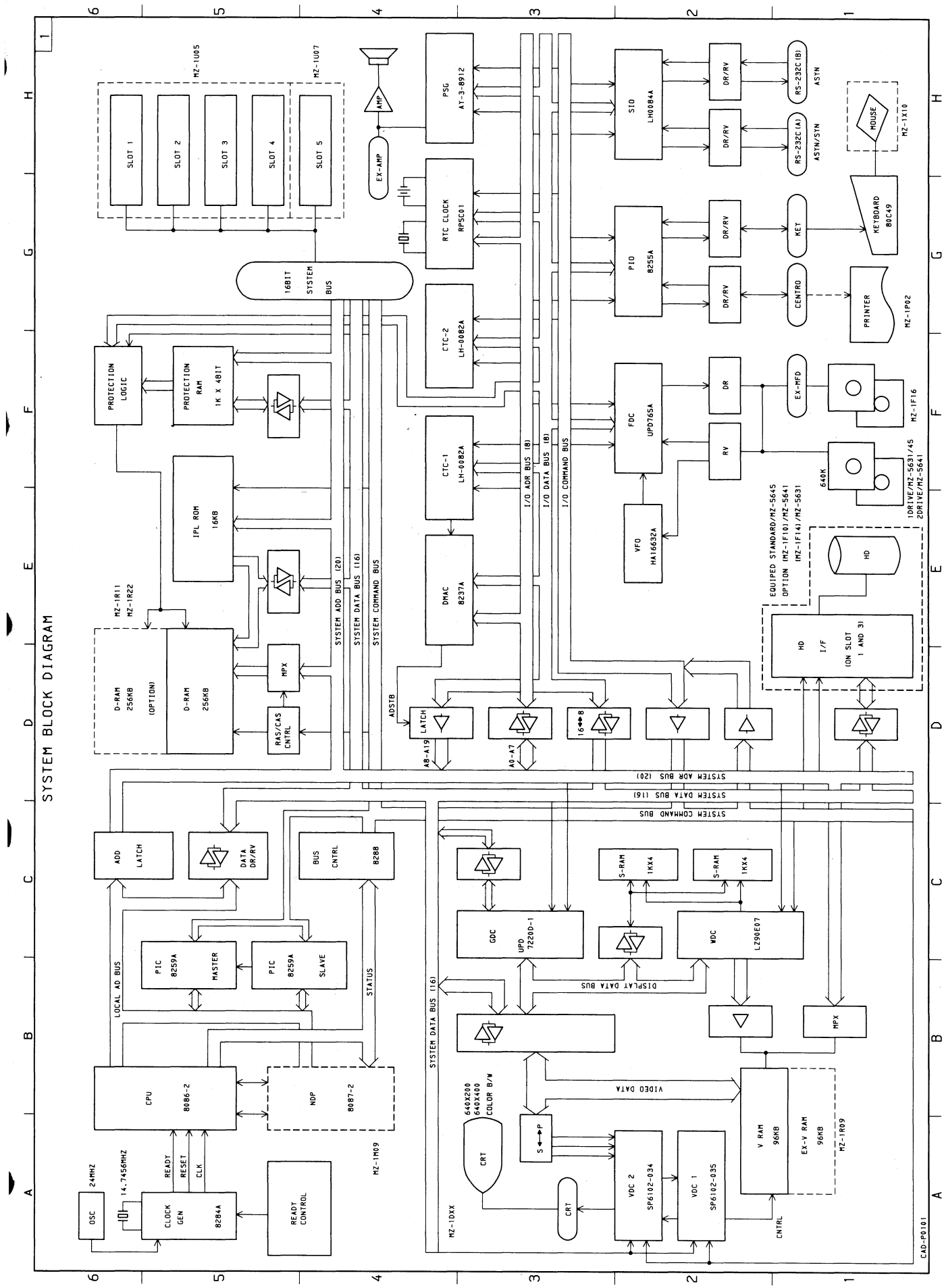
Connection table

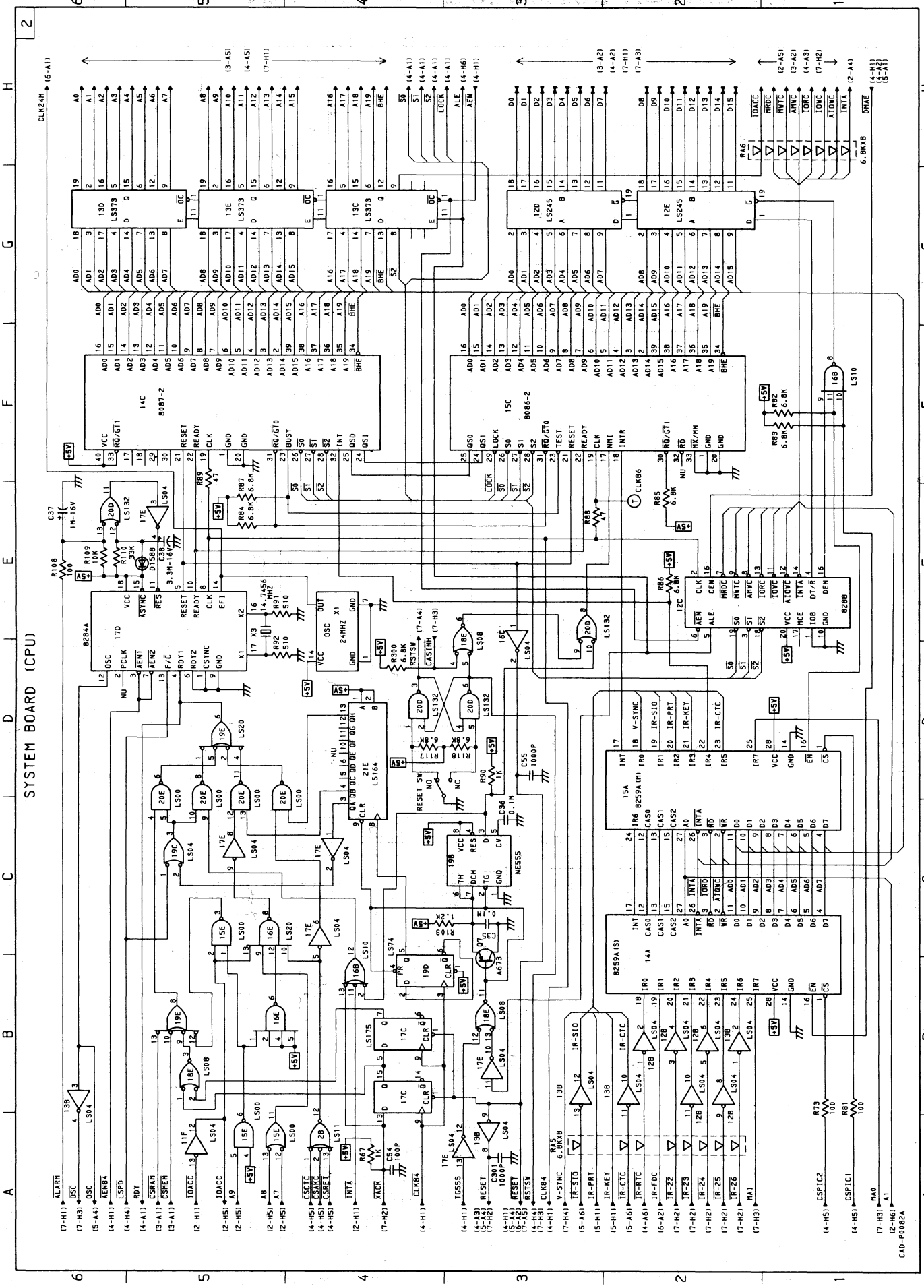
Pin No.	Wire color	
1	Gray/Black	(B)
2	Gray/Red	(B)
3	Orange/Red	(B)
4	Pink/Red	(A)
5	Yellow/Red	(A)
6	White/Red	(A)
7	Gray/Red	(A)
8	Orange/Red	(A)
9	N.C	
10	Orange/Black	(B)
11	Pink/Black	(A)
12	Yellow/Black	(A)
13	White/Black	(A)
14	Gray/Black	(A)
15	Orange/Black	(A)

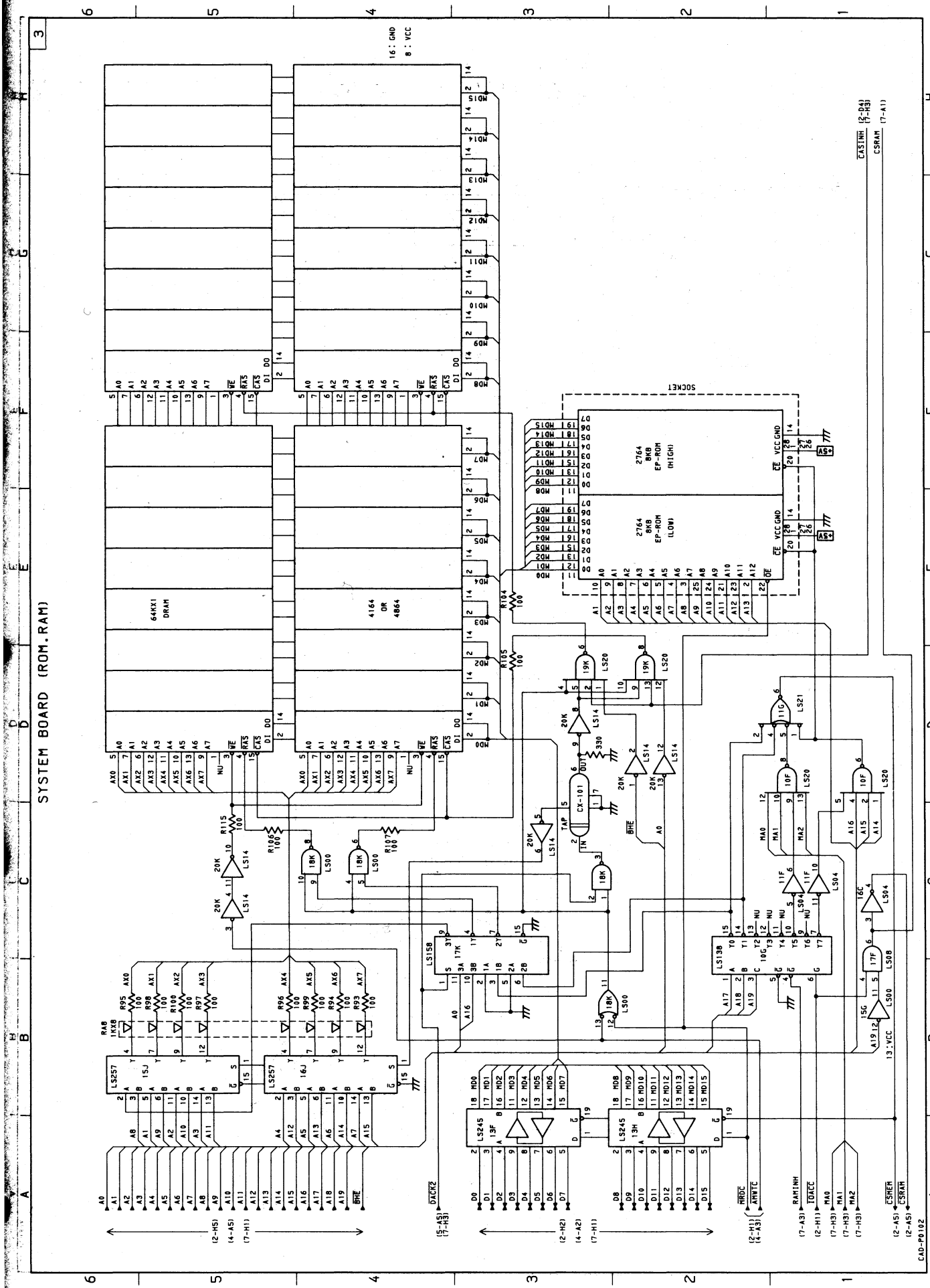


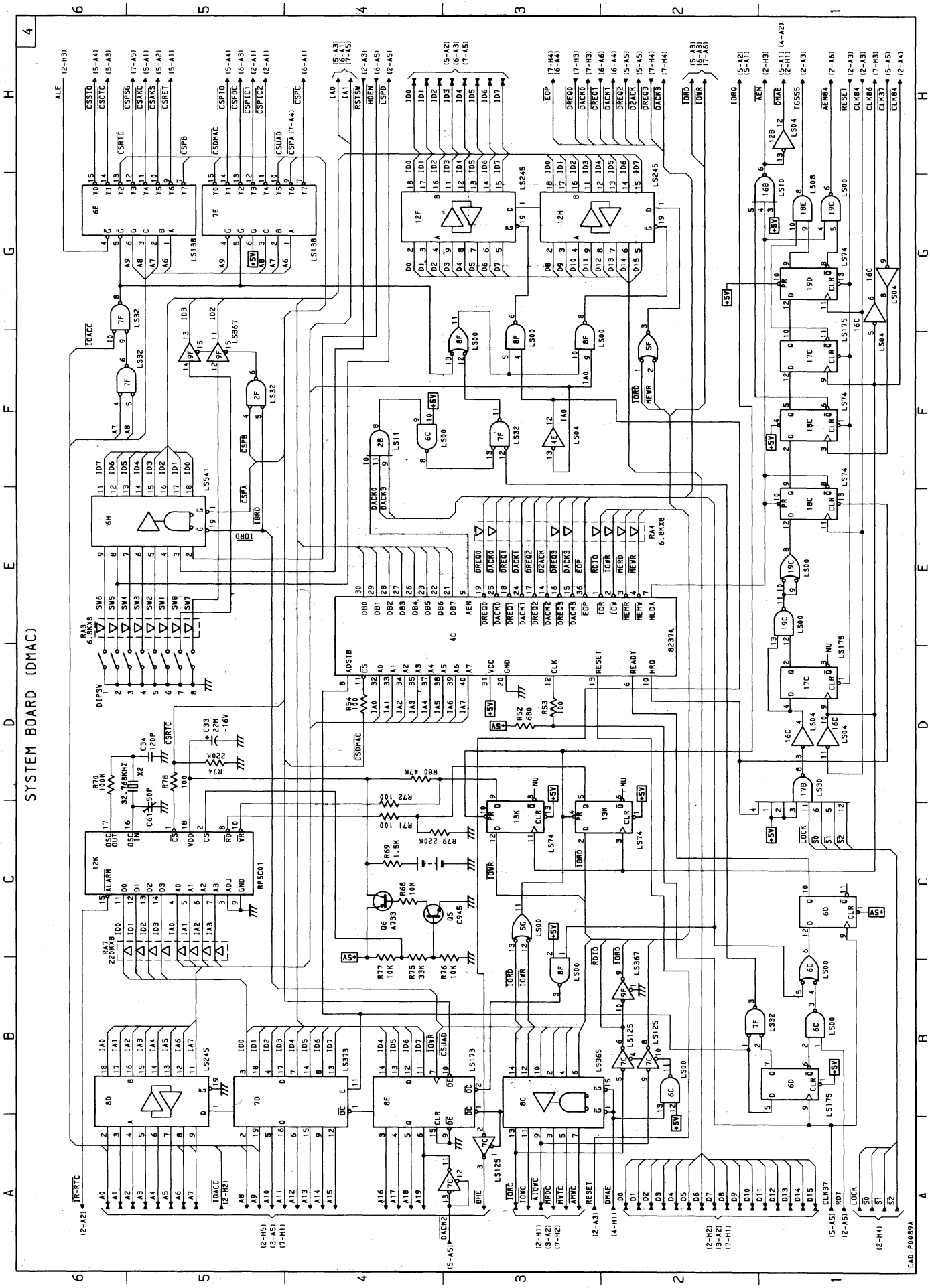
Connector A Pin No.	Wire color	Signal name	Connector B Pin No.	Connector A Pin No.	Wire color	Signal name	Connector B Pin No.
1	Orange/Red	GND	1	15	Orange/Black	ST2	15
2	Orange/Black	SD	2	–	–	–	9
3	Gray/Red	RD	3	–	–	–	10
4	White/Red	RS	4	–	–	–	11
5	White/Black	CTS	5	–	–	–	12
6	Yellow/Red	READY	–	–	–	–	13
7	Gray/Black	GND	7	–	–	–	16
8	Pink/Red	DR	6	–	–	–	17
9	Orange/Red	GND	–	–	–	–	18
10	Pink/Black	CD	8	–	–	–	19
11	Gray/Red	CI	22	–	–	–	21
12	Gray/Black	ER	20	–	–	–	23
13	–	–	–	–	–	–	24
14	Yellow/Black	RT	14	–	–	–	25

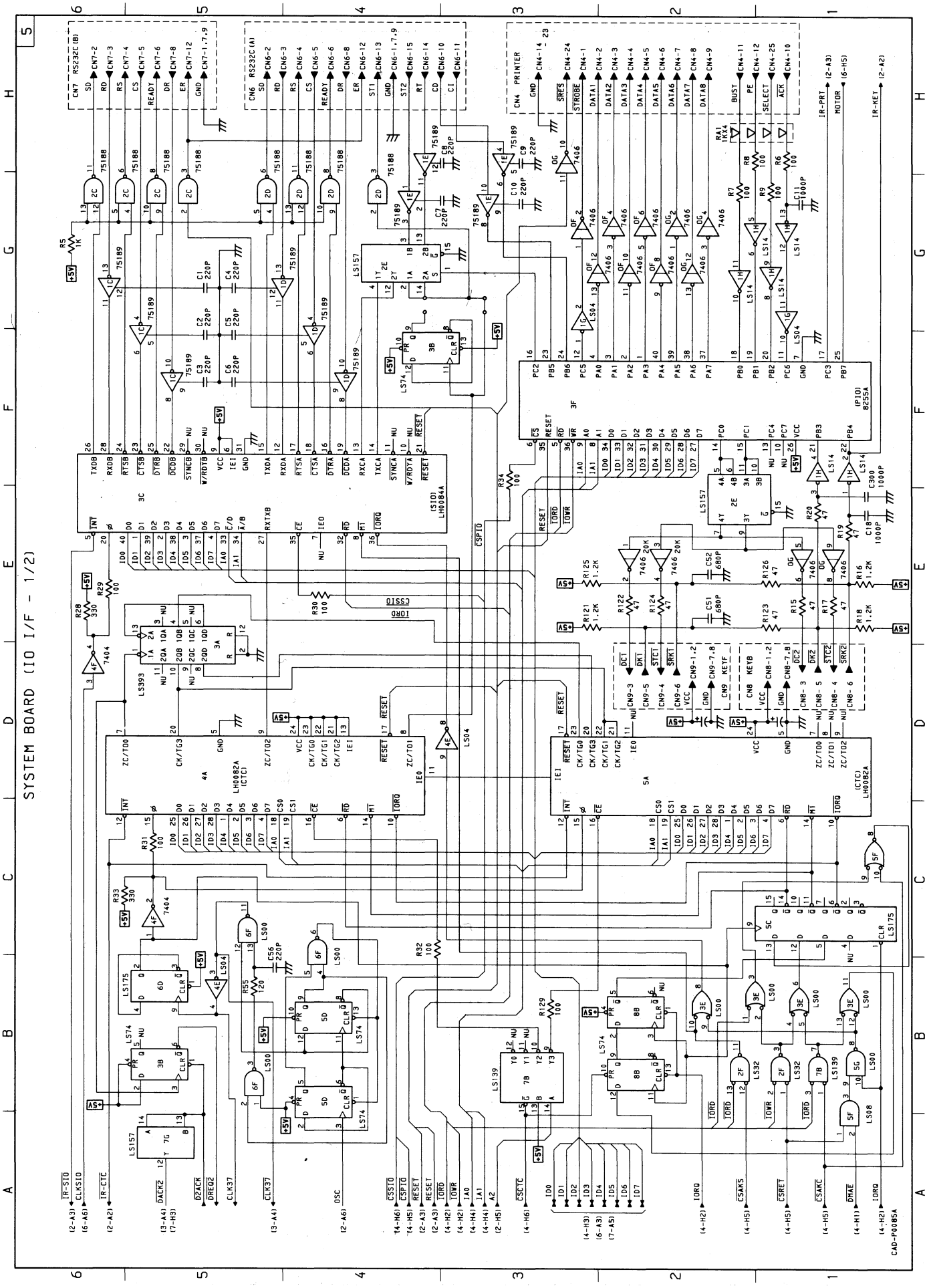
19. CIRCUIT DIAGRAM & PARTS & POSITION

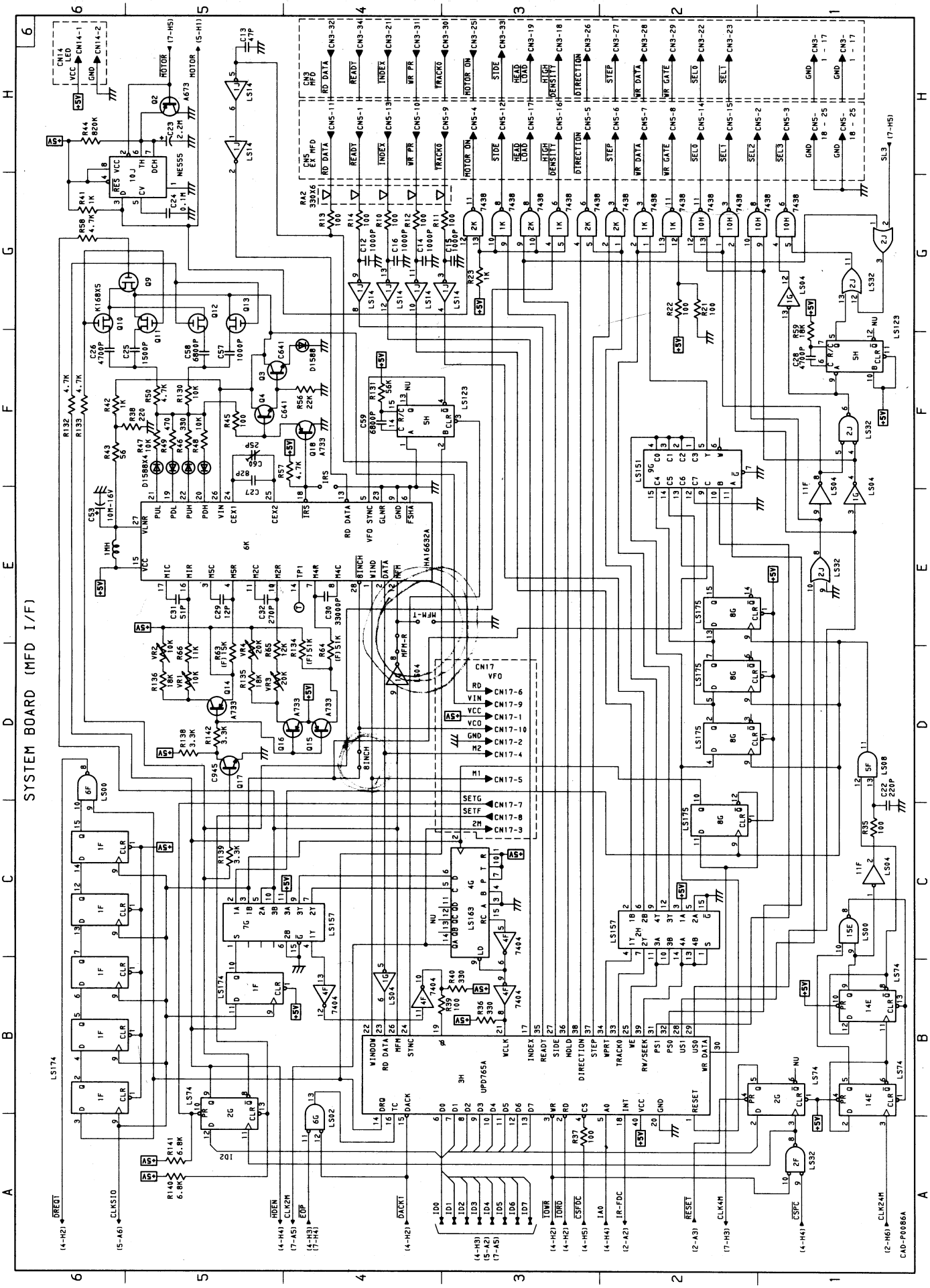


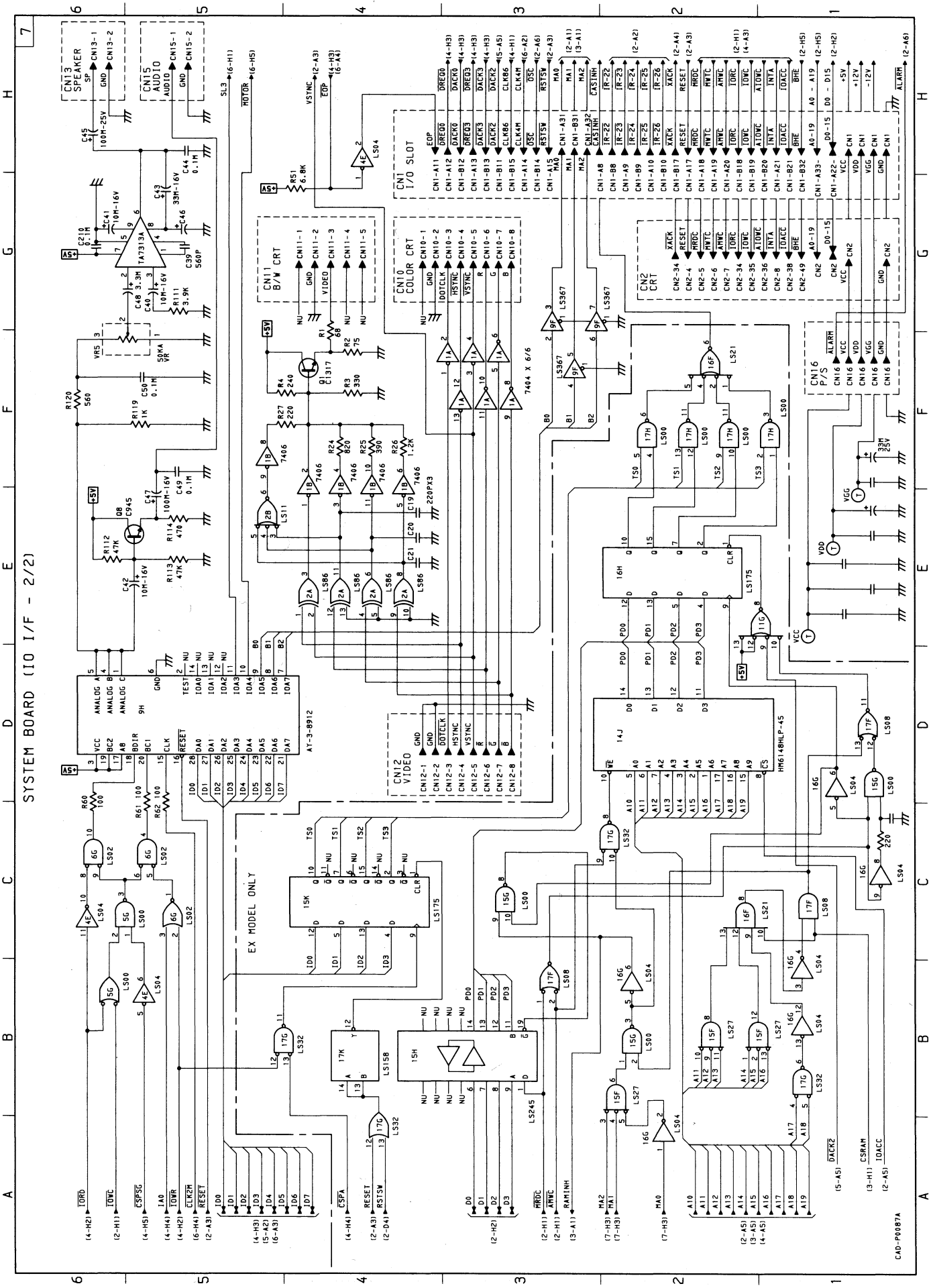












CPU BOARD (CONNECTOR)

① I/O SLOT

A		B
VCC	1	VCC
VCC	2	VCC
VDD	3	VGG
GND	4	GND
GND	5	GND
VCC	6	VCC
VCC	7	VCC
CASINH	8	IR-22
IR-23	9	IR-24
IR-25	10	IR-26
EOP	11	DACK2
DREQ0	12	DACK0
DREQ3	13	DACK3
CLK4M	14	OSC
RSTSW	15	CLK86
GND	16	GND
RESET	17	XACK
MRDC	18	IORC
MWTC	19	IOWC
AMWC	20	AIOWC
INTA	21	IOACC
D0	22	D1
D2	23	D3
D4	24	D5
D6	25	D7
D8	26	D9
D10	27	D11
D12	28	D13
D14	29	D15
GND	30	GND
MA0	31	MA1
MA2	32	BHE
A0	33	A1
A2	34	A3
A4	35	A5
A6	36	A7
A8	37	A9
A10	38	A11
A12	39	A13
A14	40	A15
A16	41	A17
A18	42	A19
GND	43	GND

② CRT

1	VCC	31	VCC
2	VCC	32	VCC
3	VCC	33	VCC
4	RESET	34	XACK
5	MRDC	35	IORC
6	MWTC	36	IOWC
7	AMWC	37	AIOWC
8	INTA	38	IOACC
9	D0	39	D1
10	D2	40	D3
11	D4	41	D5
12	D6	42	D7
13	D8	43	D9
14	D10	44	D11
15	D12	45	D13
16	D14	46	D15
17	GND	47	GND
18	GND	48	GND
19	GND	49	BHE
20	A0	50	A1
21	A2	51	A3
22	A4	52	A5
23	A6	53	A7
24	A8	54	A9
25	A10	55	A11
26	A12	56	A13
27	A14	57	A15
28	A16	58	A17
29	A18	59	A19
30	GND	60	GND

③ MFD

1	GND	18	HIGH DENSITY
2	GND	19	HEAD LOAD
3	GND	20	
4	GND	21	INDEX
5	GND	22	SEL0
6	GND	23	SEL1
7	GND	24	
8	GND	25	MOTOR ON
9	GND	26	DIRECTION
10	GND	27	STEP
11	GND	28	WR DATA
12	GND	29	WR GATE
13	GND	30	TRACK0
14	GND	31	WR PR
15	GND	32	RD DATA
16	GND	33	SIDE
17	GND	34	READY

④ EX-MFD

1	INDEX	14	SEL0
2	SEL2	15	SEL1
3	SEL3	16	HIGH DENSITY
4	MOTOR ON	17	HEAD LOAD
5	DIRECTION	18	GND
6	STEP	19	GND
7	WR DATA	20	GND
8	WR GATE	21	GND
9	TRACK0	22	GND
10	WR PR	23	GND
11	RD DATA	24	GND
12	SIDE	25	
13	READY		

⑤ PRINTER

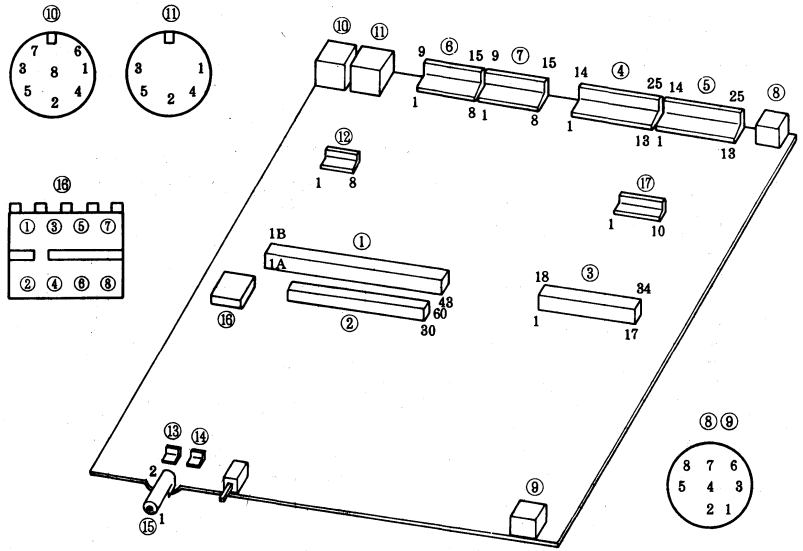
1	STROBE	14	GND
2	DATA1	15	GND
3	DATA2	16	GND
4	DATA3	17	GND
5	DATA4	18	GND
6	DATA5	19	GND
7	DATA6	20	GND
8	DATA7	21	GND
9	DATA8	22	GND
10	ACK	23	GND
11	BUSY	24	SRES
12	PE	25	SELECT
13			

⑥ RS-232C (B)

1	GND	9	GND
2	SD	10	
3	RD	11	
4	RS	12	ER
5	CS	13	
6	READY	14	
7	GND	15	
8	DR		

⑦ RS-232C (A)

1	GND	9	GND
2	SD	10	CD
3	RD	11	CI
4	RS	12	ER
5	CS	13	ST1
6	READY	14	RT
7	GND	15	ST2
8	DR		



⑧ KEY2

1	VCC
2	VCC
3	DC2
4	STC2
5	DK2
6	SRK2
7	GND
8	GND

⑨ KEY1

1	VCC
2	VCC
3	DC1
4	STC1
5	DK1
6	SRK1
7	GND
8	GND

⑩ COLOR CRT

1	
2	GND
3	DOTCLK
4	HSYNC
5	VSYNC
6	R
7	G
8	B

⑫ VIDEO

1	GND
2	GND
3	DOTCLK
4	HSYNC
5	VSYNC
6	R
7	G
8	B

⑪ B/W CRT

1	
2	GND
3	VIDEO
4	
5	

⑭ LED

1	LED
2	GND

⑮ AUDIO

1	AUDIO
2	GND

⑰ VFO

1	VCC
2	GND
3	CLK2M
4	M1
5	M2
6	RD
7	SETG
8	SETF
9	VIN
10	VCO

⑯ P/S

1	VGG	2	VDD
3	VCC	4	VCC
5	ALARM	6	GND
7	GND	8	GND

⑬ SPEAKER

1	SP
2	GND

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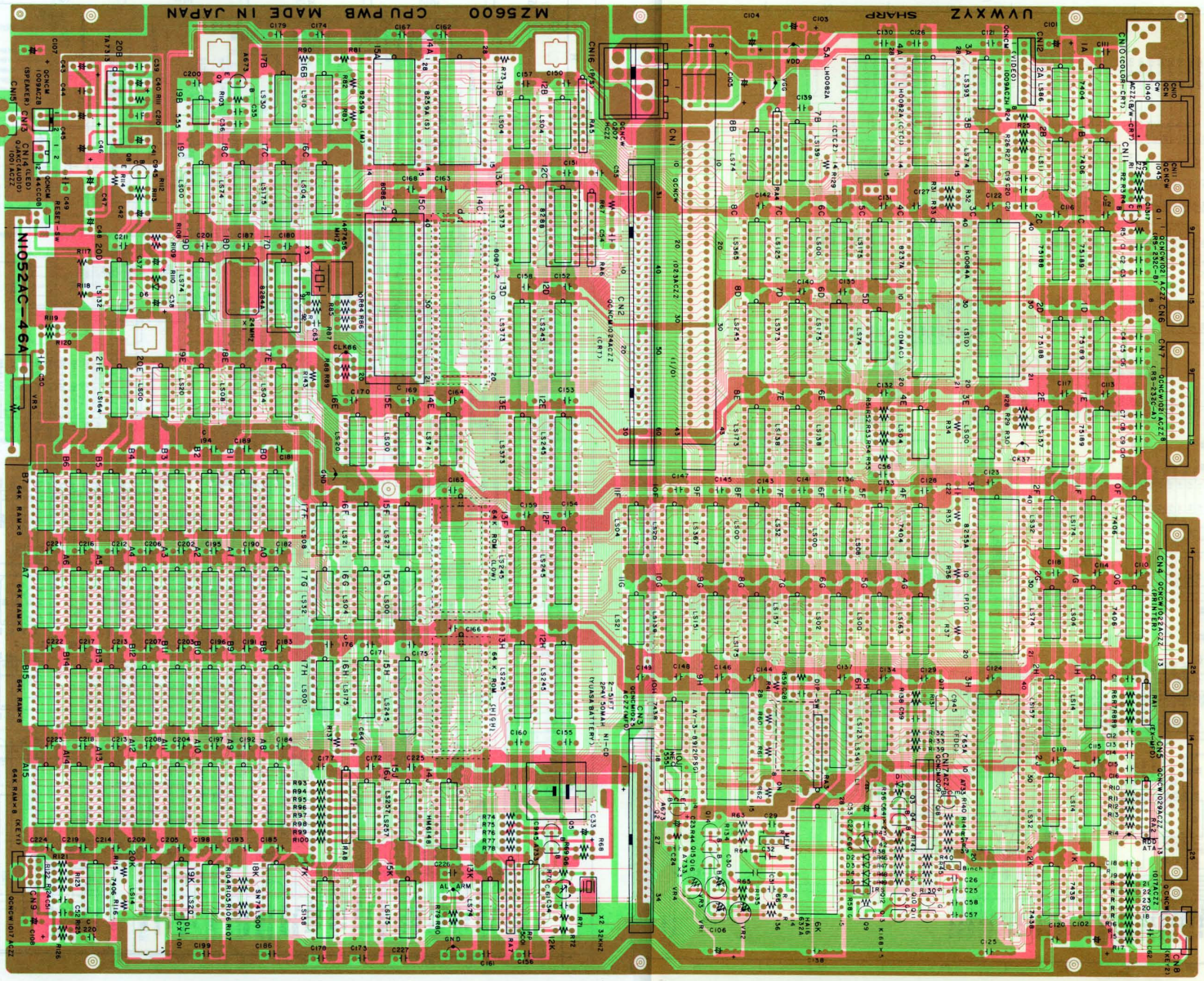
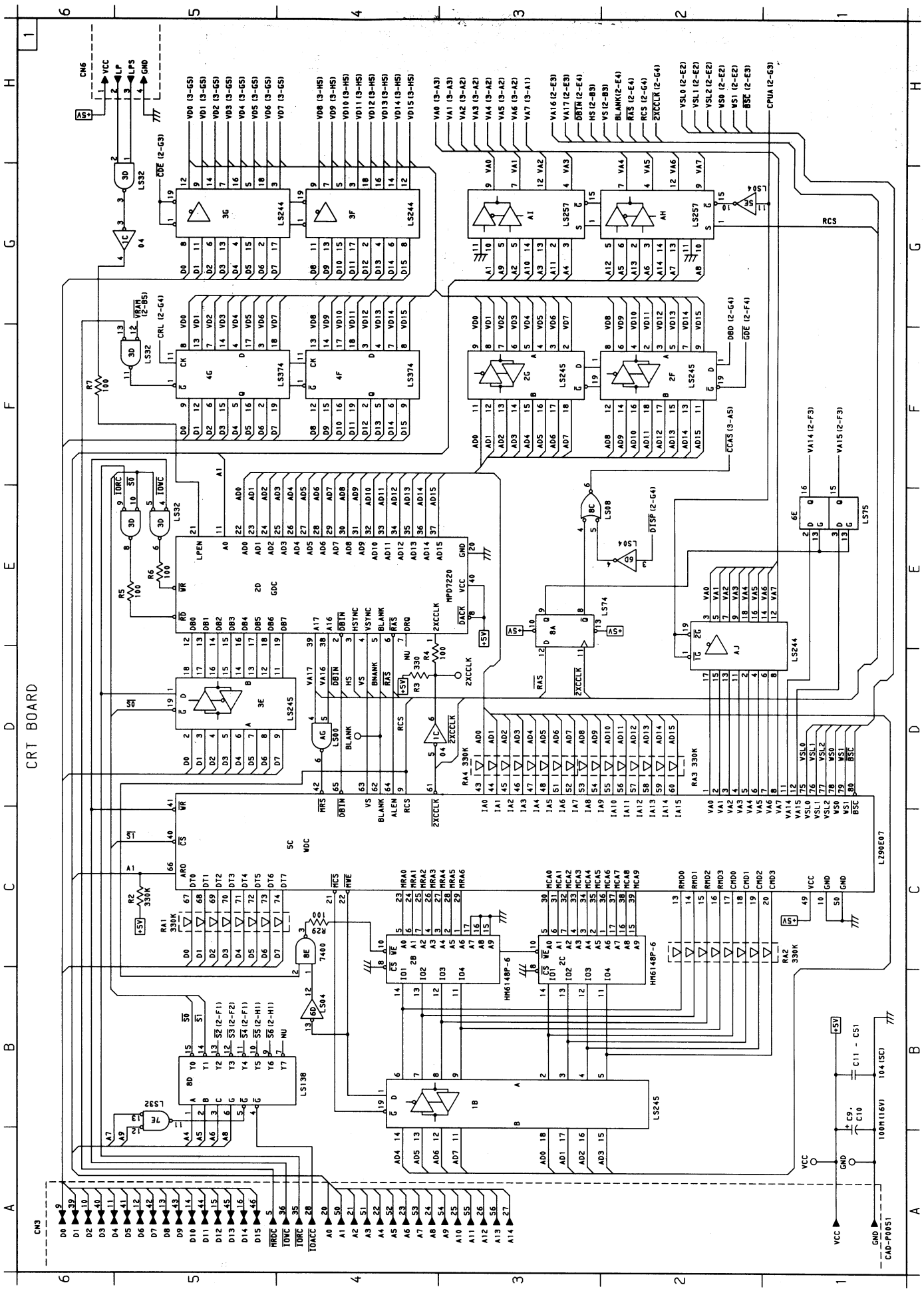
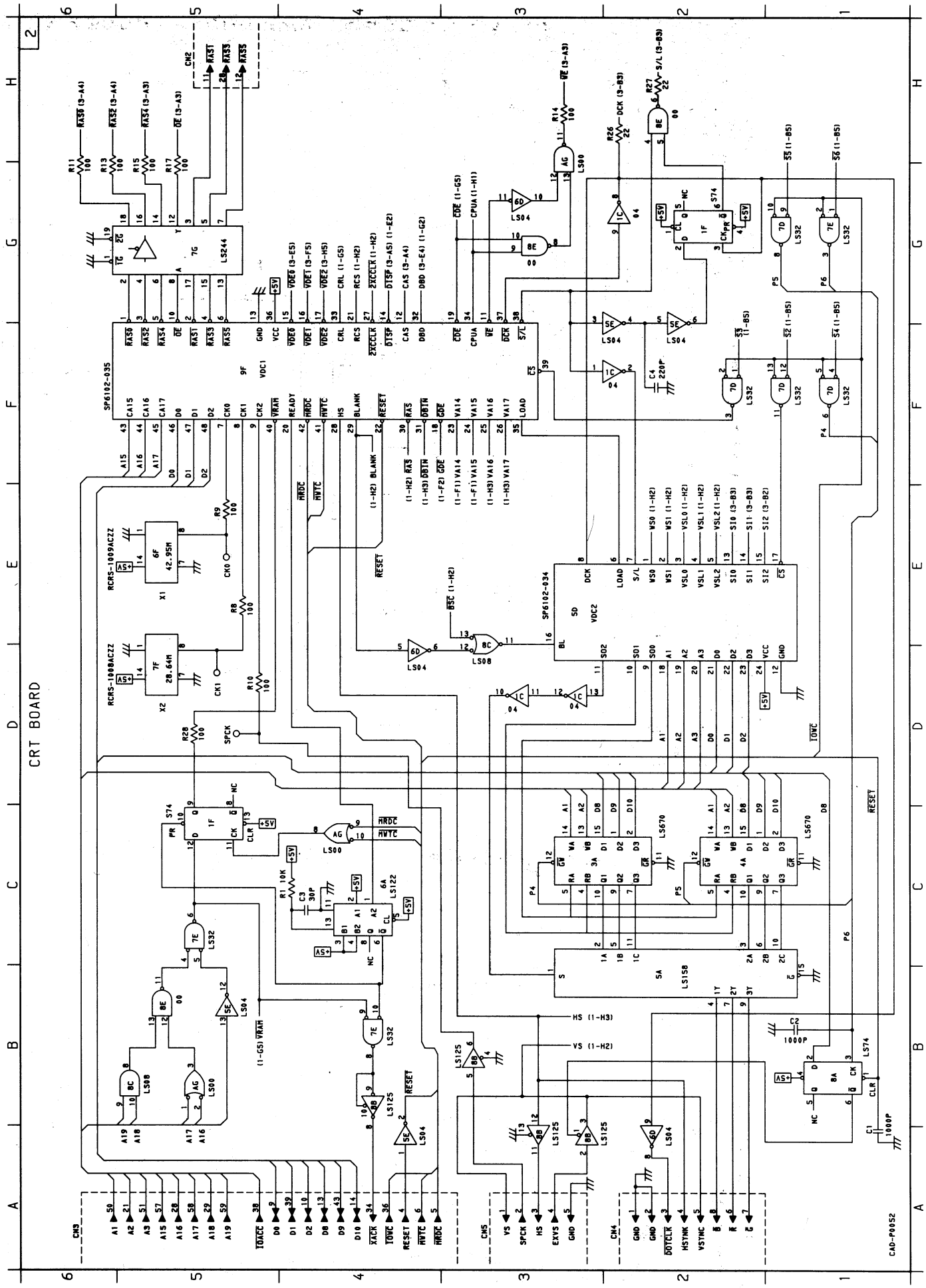
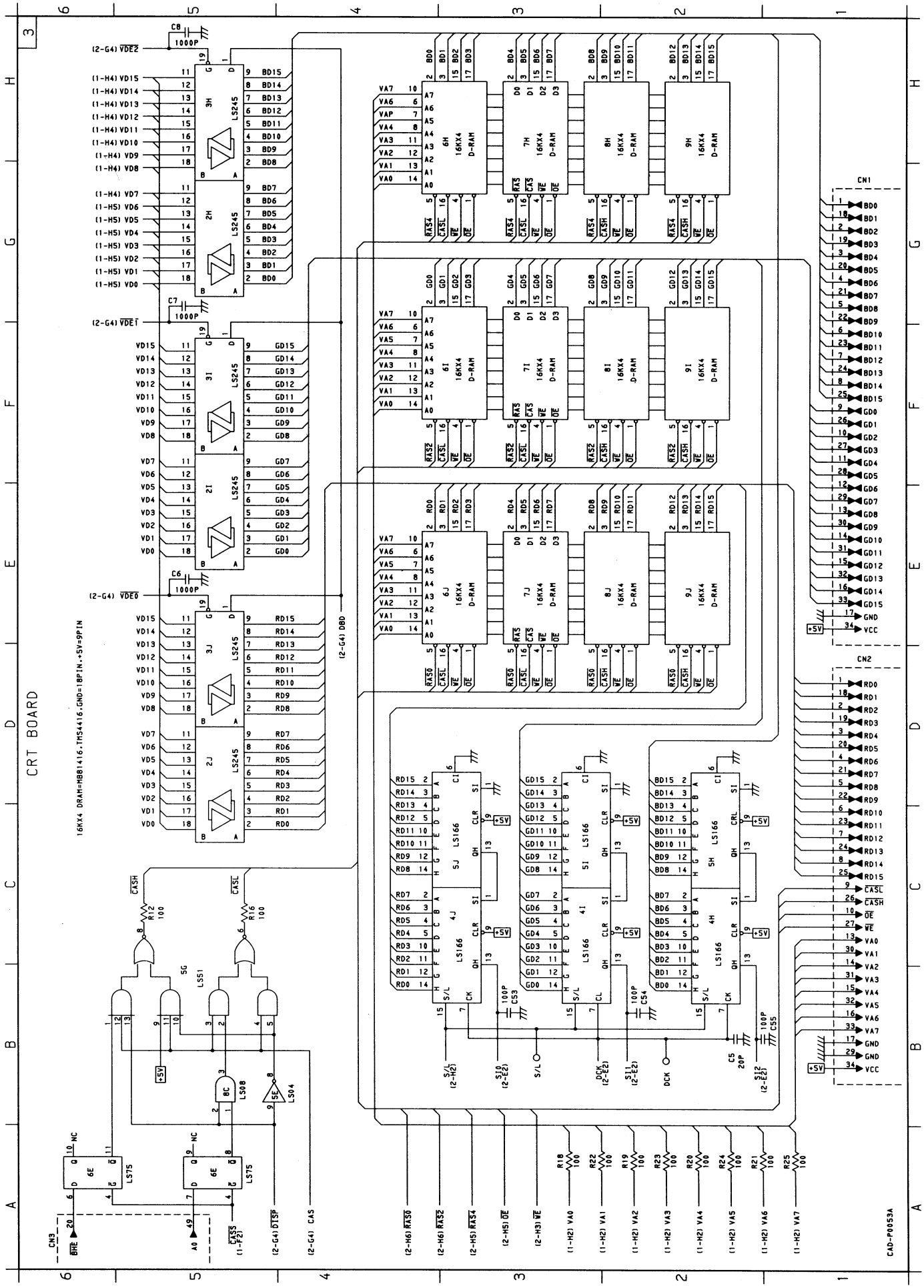
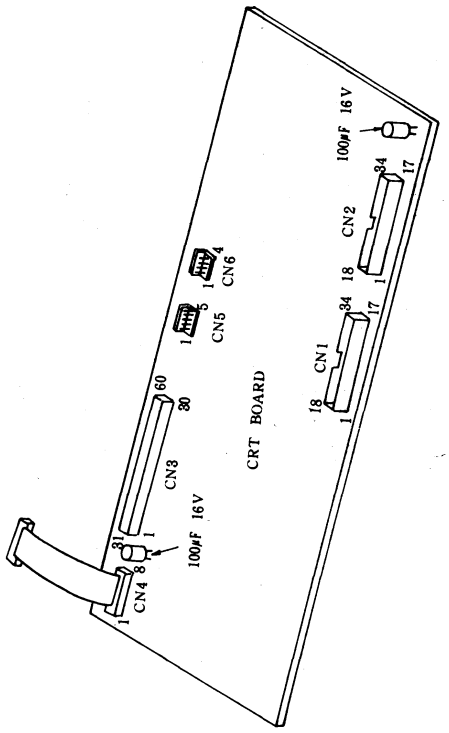
MZ-5600











CRT BOARD

CN1 QCNCH1026ACZZ

1	BD0	18	BD1
2	BD2	19	BD3
3	BD4	20	BD5
4	BD6	21	BD7
5	BD8	22	BD9
6	BD10	23	BD11
7	BD12	24	BD13
8	BD14	25	BD15
9	GD0	26	GD1
10	GD2	27	GD3
11	GD4	28	GD5
12	GD6	29	GD7
13	GD8	30	GD9
14	GD10	31	GD11
15	GD12	32	GD13
16	GD14	33	GD15
17	GND	34	VCC (5V)

CN2 QCNCH1026ACZZ

1	RD0	18	RD1
2	RD2	19	RD3
3	RD4	20	RD5
4	RD6	21	RD7
5	RD8	22	RD9
6	RD10	23	RD11
7	RD12	24	RD13
8	RD14	25	RD15
9	CASL	26	CASH
10	OE	27	WE
11	RAS1	28	RAS3
12	RAS5	29	GND
13	VA0	30	VA1
14	VA2	31	VA3
15	VA4	32	VA5
16	VA6	33	VA7
17	GND	34	VCC (5V)

CN3 QCNCH1027ACZZ

1	VCC (5V)	31	VCC (5V)
2	VCC (5V)	32	VCC (5V)
3	VCC (5V)	33	VCC (5V)
4	RESET	34	XACK
5	MRDC	35	IORC
6	MWTC	36	IOWC
7	AMWC	37	AIOWC
8	INTA	38	IOACC
9	D0	39	D1
10	D2	40	D3
11	D4	41	D5
12	D6	42	D7
13	D8	43	D9
14	D10	44	D11
15	D12	45	D13
16	D14	46	D15
17	GND	47	GND
18	GND	48	GND
19	GND	49	BHE
20	A0	50	A1
21	A2	51	A3
22	A4	52	A5
23	A6	53	A7
24	A8	54	A9
25	A10	55	A11
26	A12	56	A13
27	A14	57	A15
28	A16	58	A17
29	A18	59	A19
30	GND	60	GND

CN4 QCNW-1055ACZZ

1	GND
2	GND
3	DOTCLK
4	HSYNC
5	VSYNC
6	R
7	G
8	B

CN5 QCNCH1009ACZE

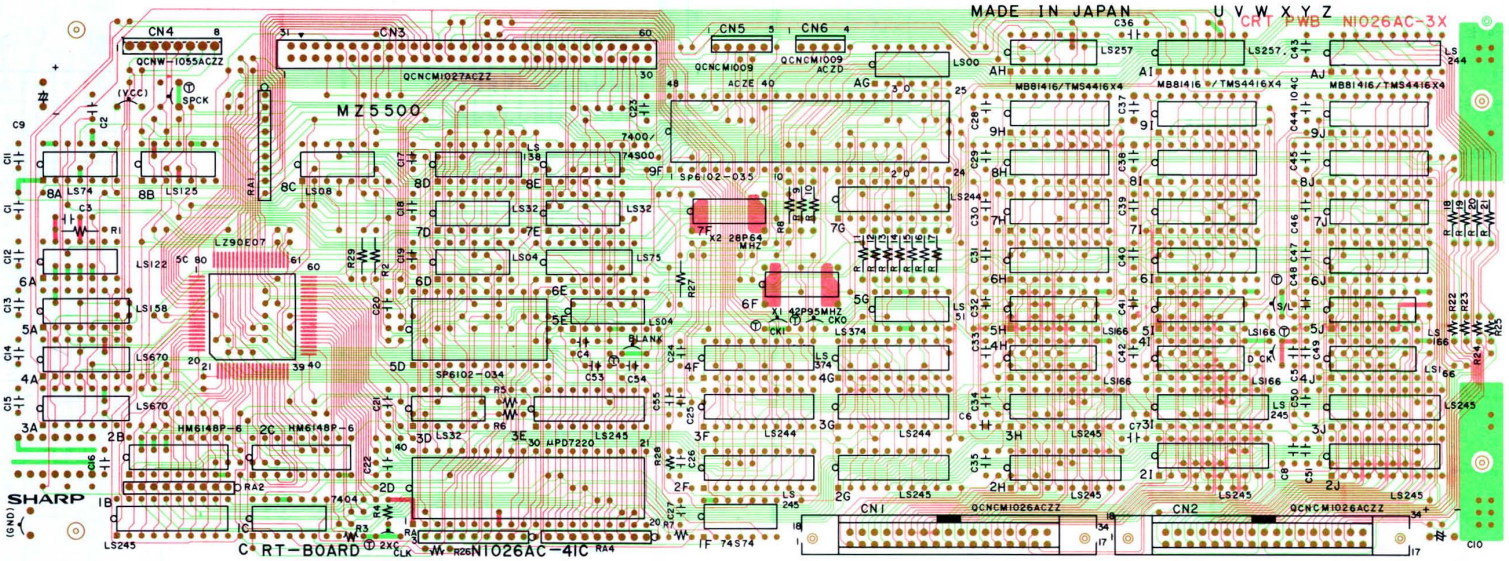
1	VS
2	SPCK
3	HS
4	EXVS
5	GND

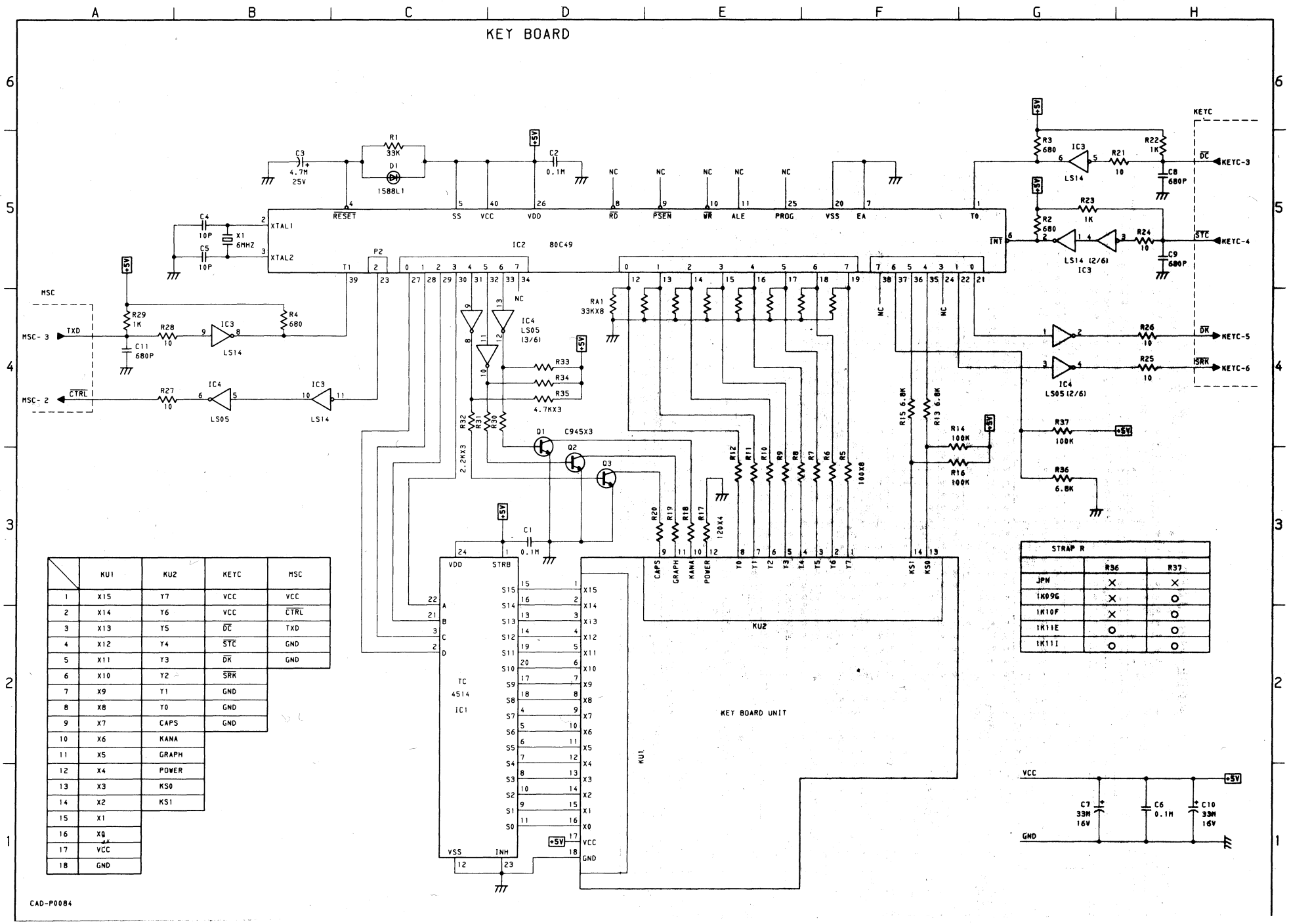
CN6 QCNCH1009ACZD

1	VCC (5V)
2	LP
3	LPS
4	GND

CAD-P0054

CRT BOARD LAYOUT

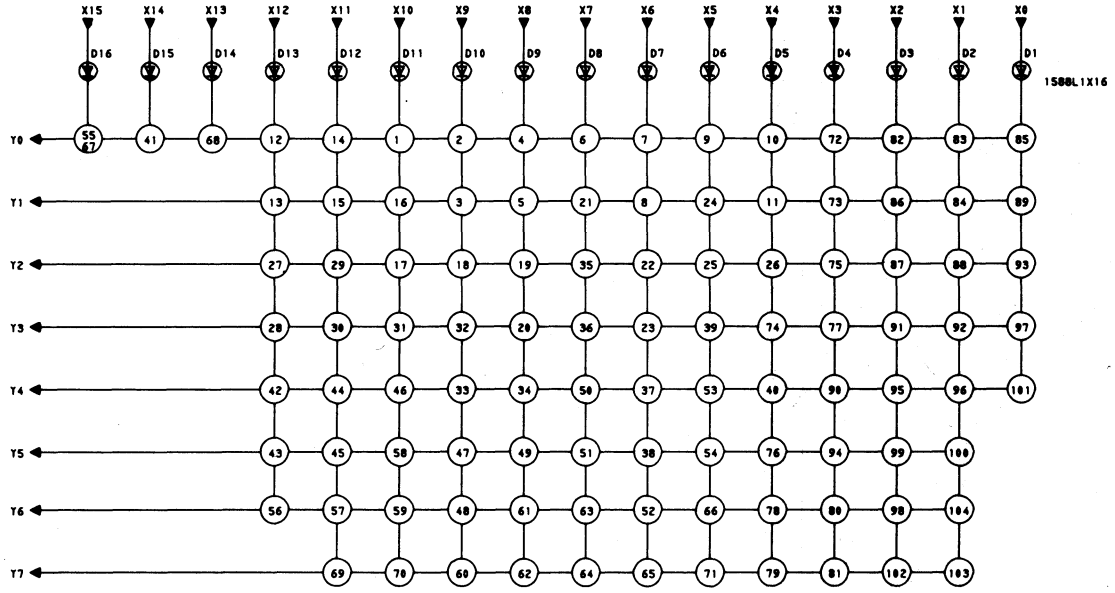




	KU1	KU2	KEYC	MSC
1	X15	Y7	VCC	VCC
2	X14	Y6	VCC	$\overline{CTRL}$
3	X13	Y5	$\overline{DC}$	TXD
4	X12	Y4	$\overline{STC}$	GND
5	X11	Y3	$\overline{DK}$	GND
6	X10	Y2	$\overline{SRK}$	
7	X9	Y1	GND	
8	X8	Y0	GND	
9	X7	CAPS	GND	
10	X6	KANA		
11	X5	GRAPH		
12	X4	POWER		
13	X3	KS0		
14	X2	KS1		
15	X1			
16	X0			
17	VCC			
18	GND			

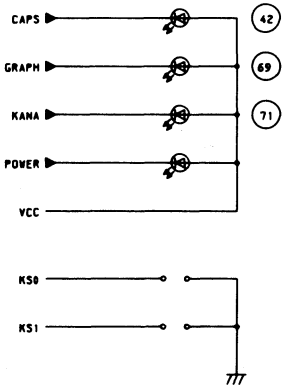
STRAP R		
	R36	R37
JPN	×	×
1K09G	×	○
1K10F	×	○
1K11E	○	○
1K11I	○	○

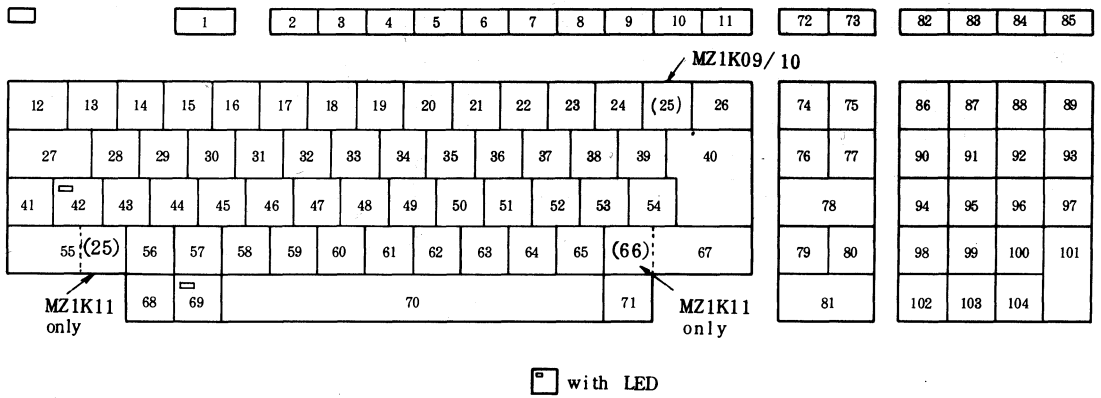
KEY MATRIX



KU1	
1	X15
2	X14
3	X13
4	X12
5	X11
6	X10
7	X9
8	X8
9	X7
10	X6
11	X5
12	X4
13	X3
14	X2
15	X1
16	X0
17	VCC (+5V)
18	GND

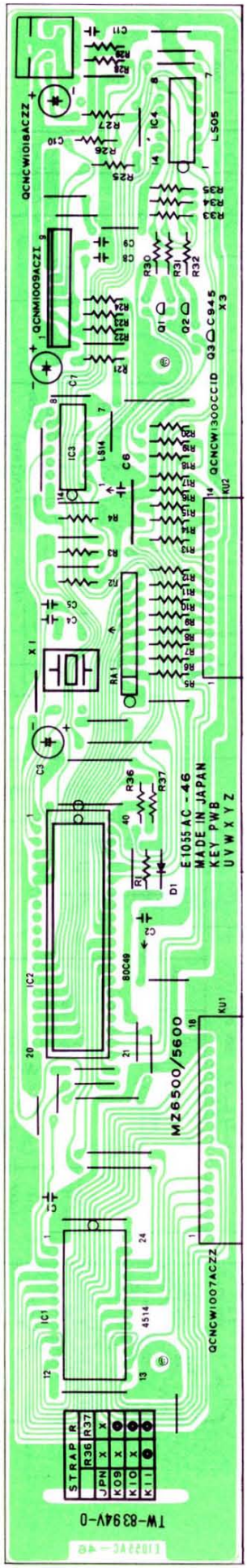
KU2	
1	Y7
2	Y6
3	Y5
4	Y4
5	Y3
6	Y2
7	Y1
8	Y0
9	CAPS
10	KANA
11	GRAPH
12	POWER
13	KS0
14	KS1

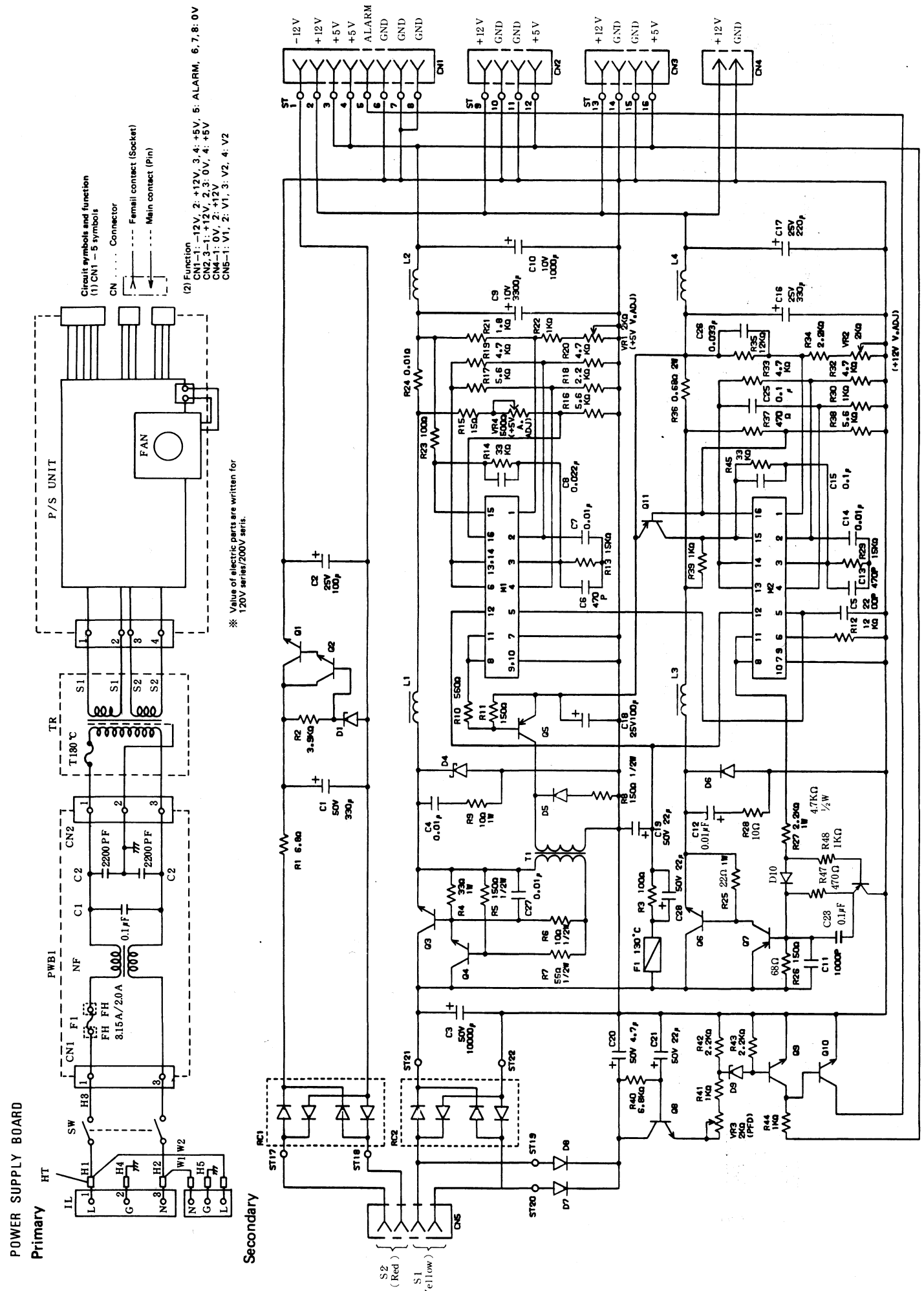




CAD-P0042

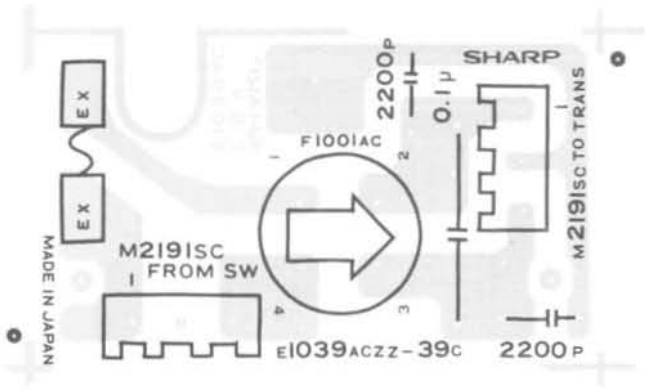
KEY BOARD LAYOUT



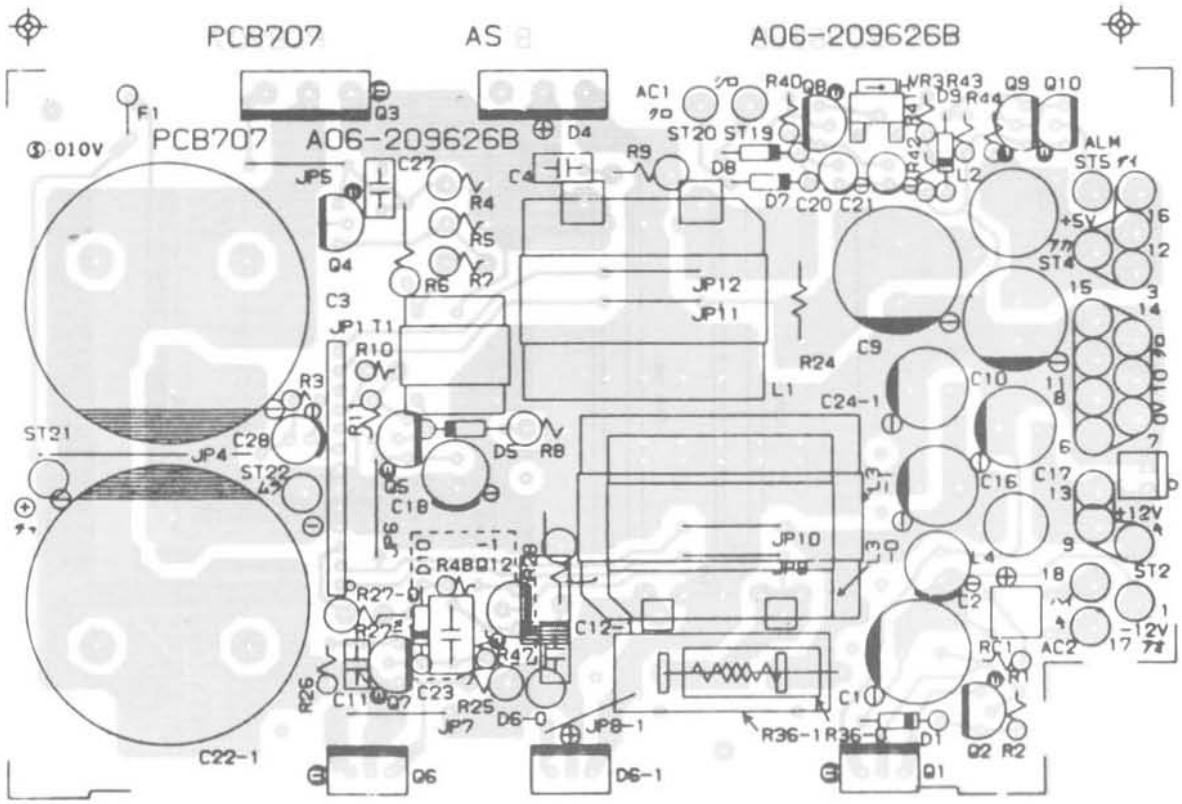


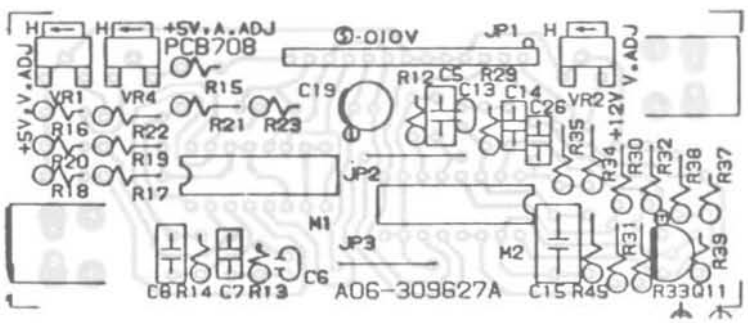
POWER SUPPLY BOARD LAYOUT

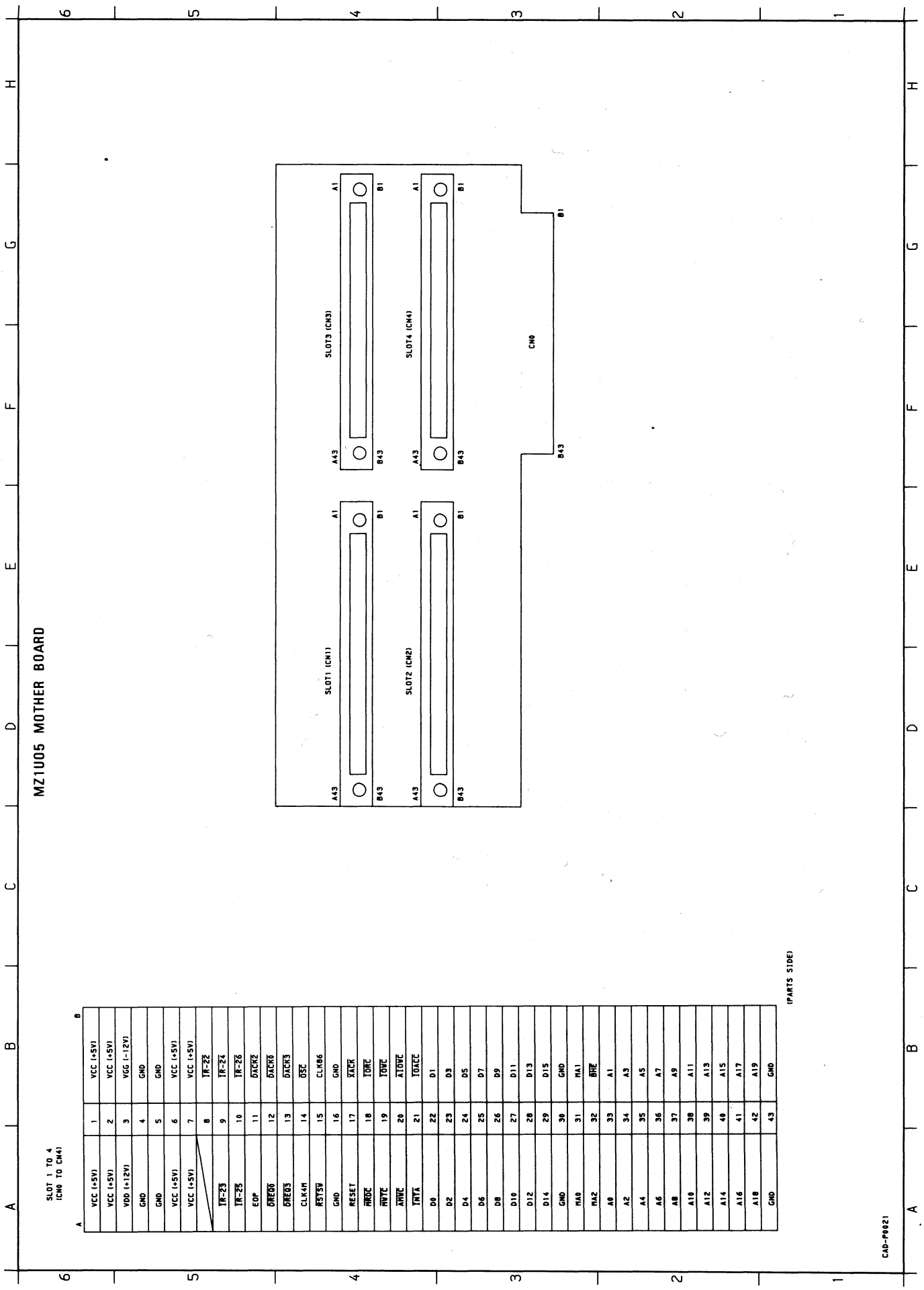
Primary



Secondary

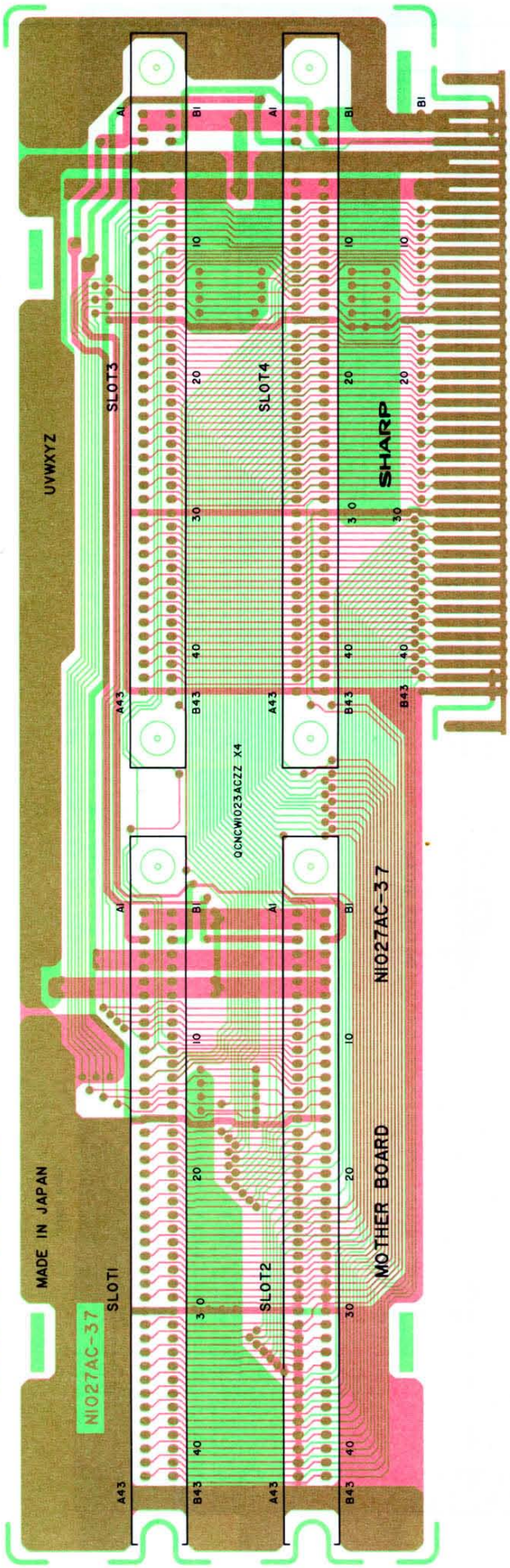


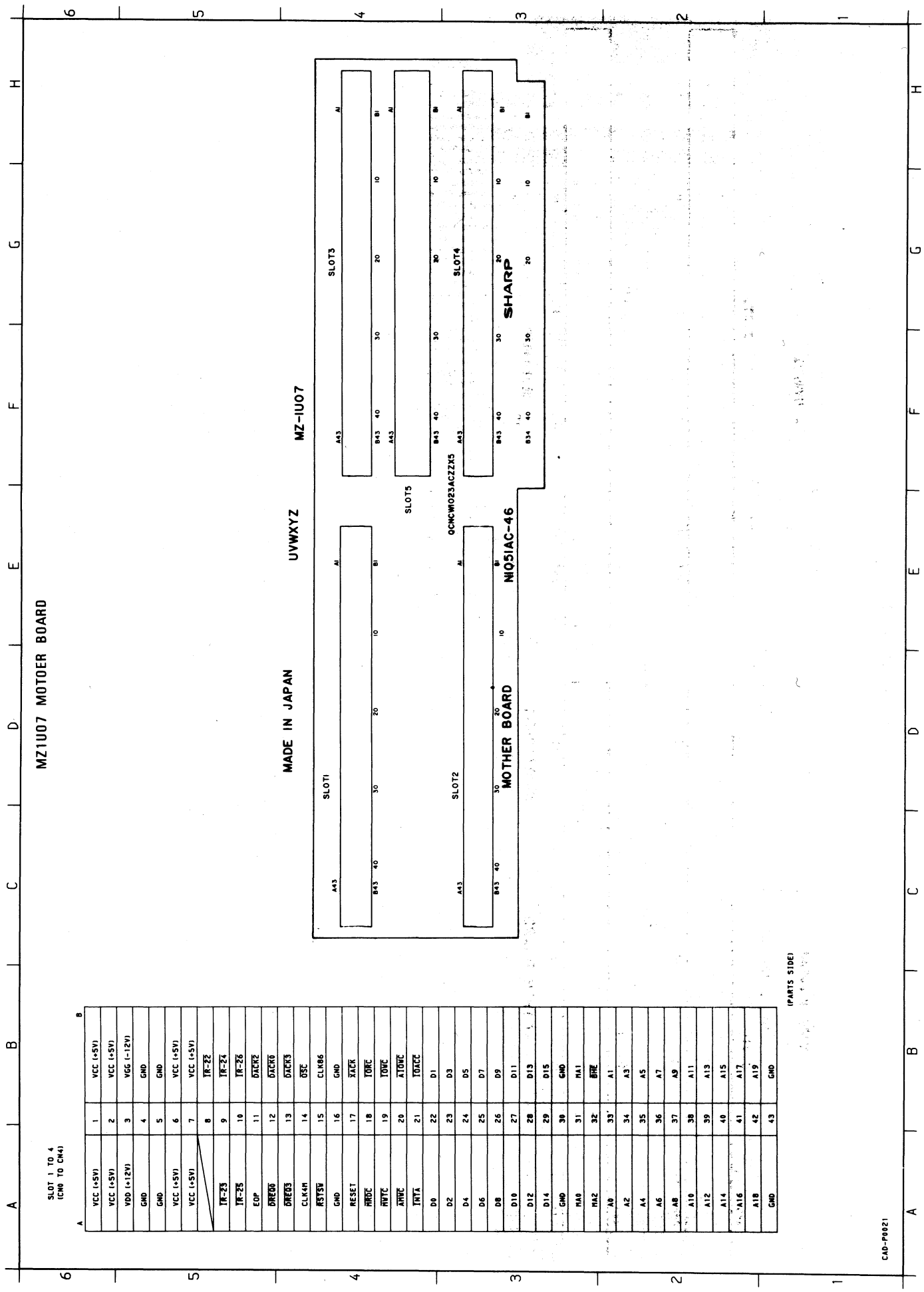




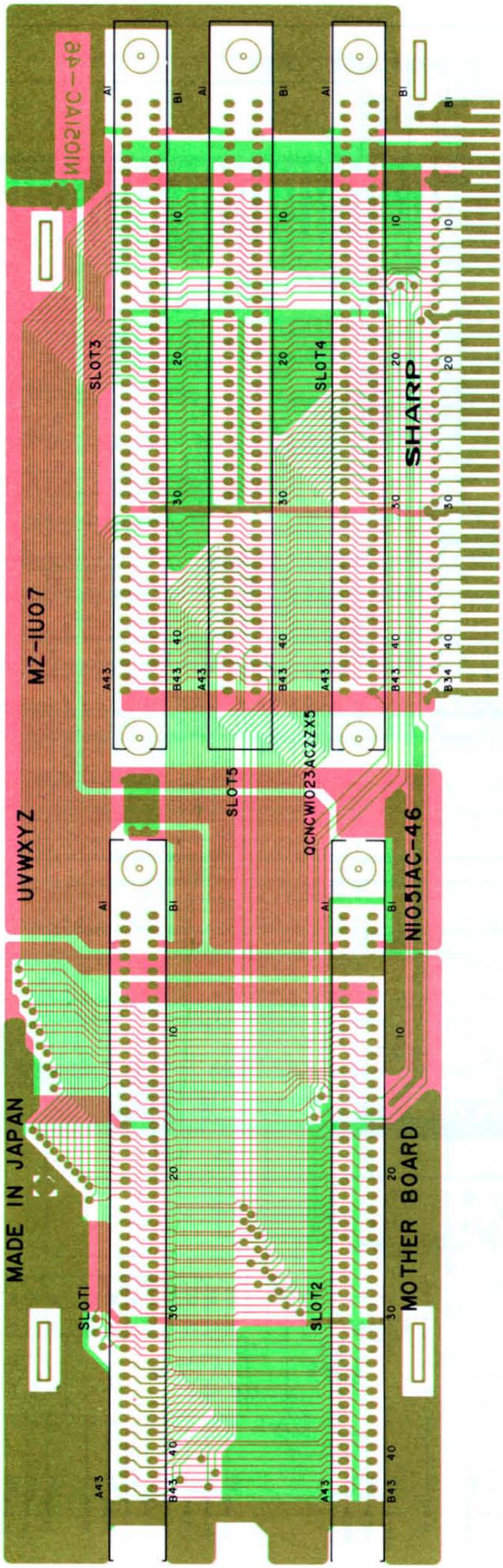
A		B
VCC (+5V)	1	VCC (+5V)
VCC (+5V)	2	VCC (+5V)
VDD (+12V)	3	VGG (-12V)
GND	4	GND
GND	5	GND
VCC (+5V)	6	VCC (+5V)
VCC (+5V)	7	VCC (+5V)
	8	IR-22
IR-23	9	IR-24
IR-25	10	IR-26
EOP	11	DACK2
DREQ0	12	DACK0
DREQ3	13	DACK3
CLK4M	14	OSC
RSTSW	15	CLK86
GND	16	GND
RESET	17	XACK
MRDC	18	TORC
MWTC	19	TOWC
AMWC	20	AIOWC
INTA	21	IOACC
D0	22	D1
D2	23	D3
D4	24	D5
D6	25	D7
D8	26	D9
D10	27	D11
D12	28	D13
D14	29	D15
GND	30	GND
MA0	31	MA1
MA2	32	BHE
A0	33	A1
A2	34	A3
A4	35	A5
A6	36	A7
A8	37	A9
A10	38	A11
A12	39	A13
A14	40	A15
A16	41	A17
A18	42	A19
GND	43	GND

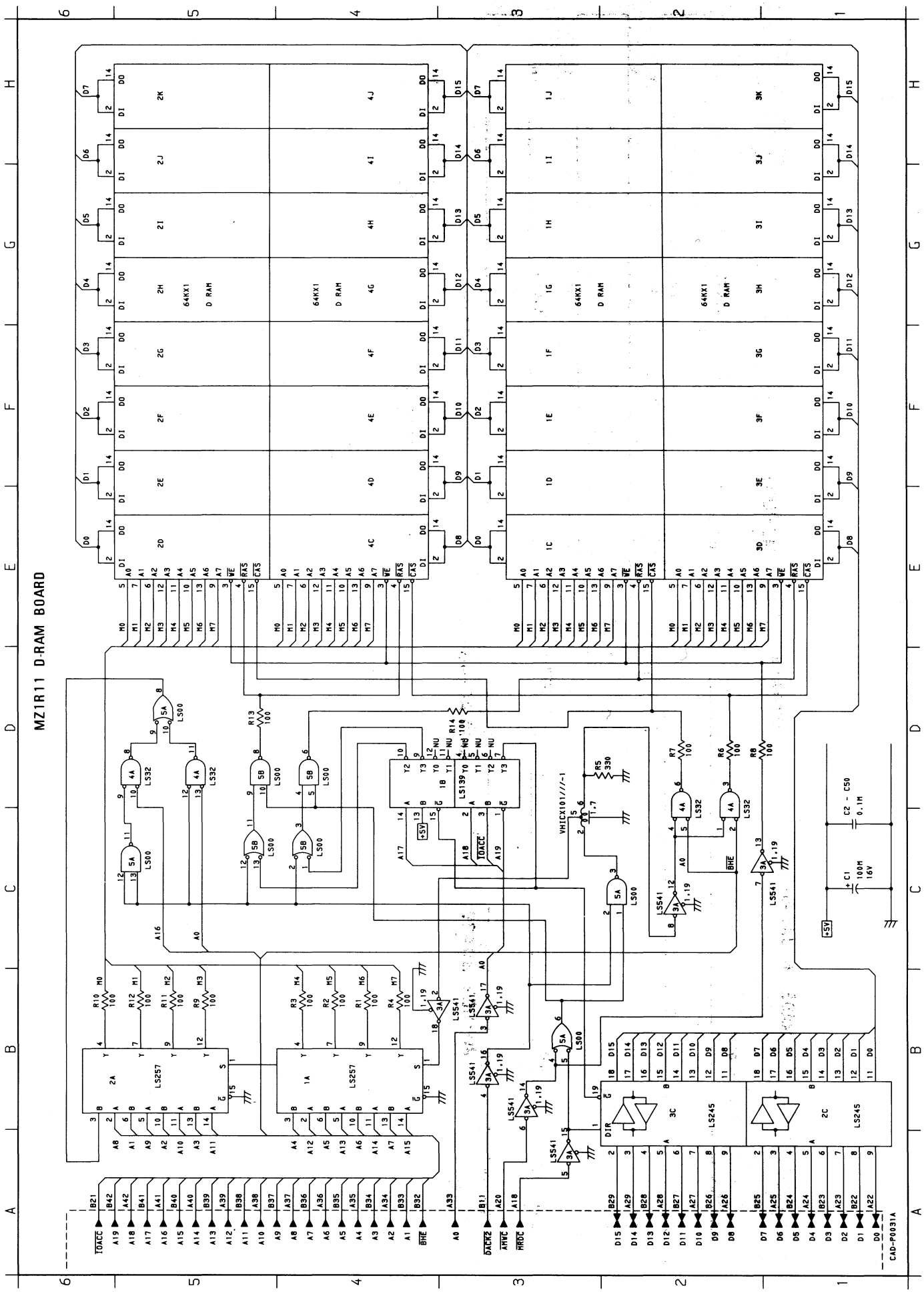
MZ1U05 MOTHER BOARD LAYOUT



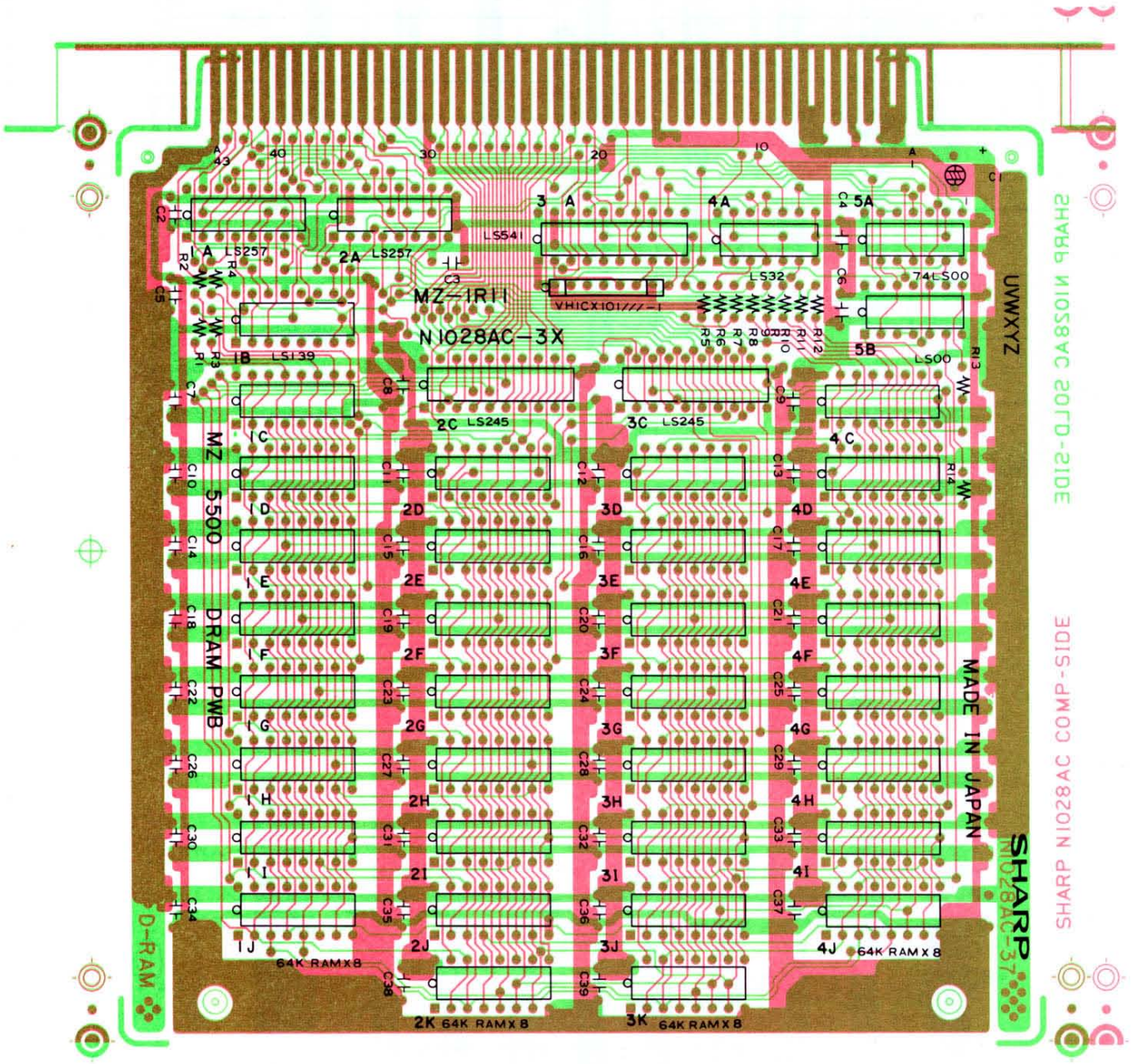


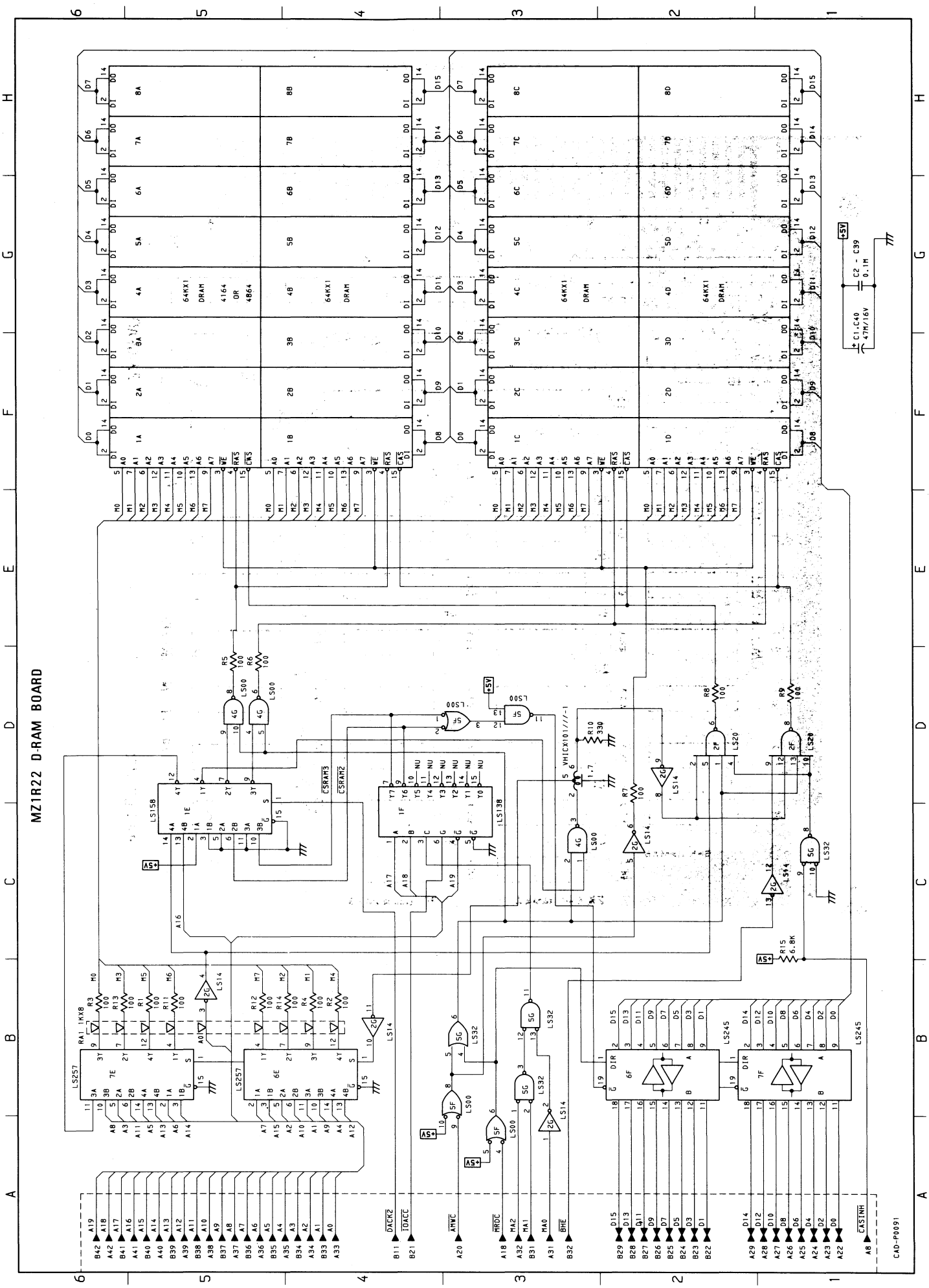
MZ1U07 MOTHER BOARD LAYOUT



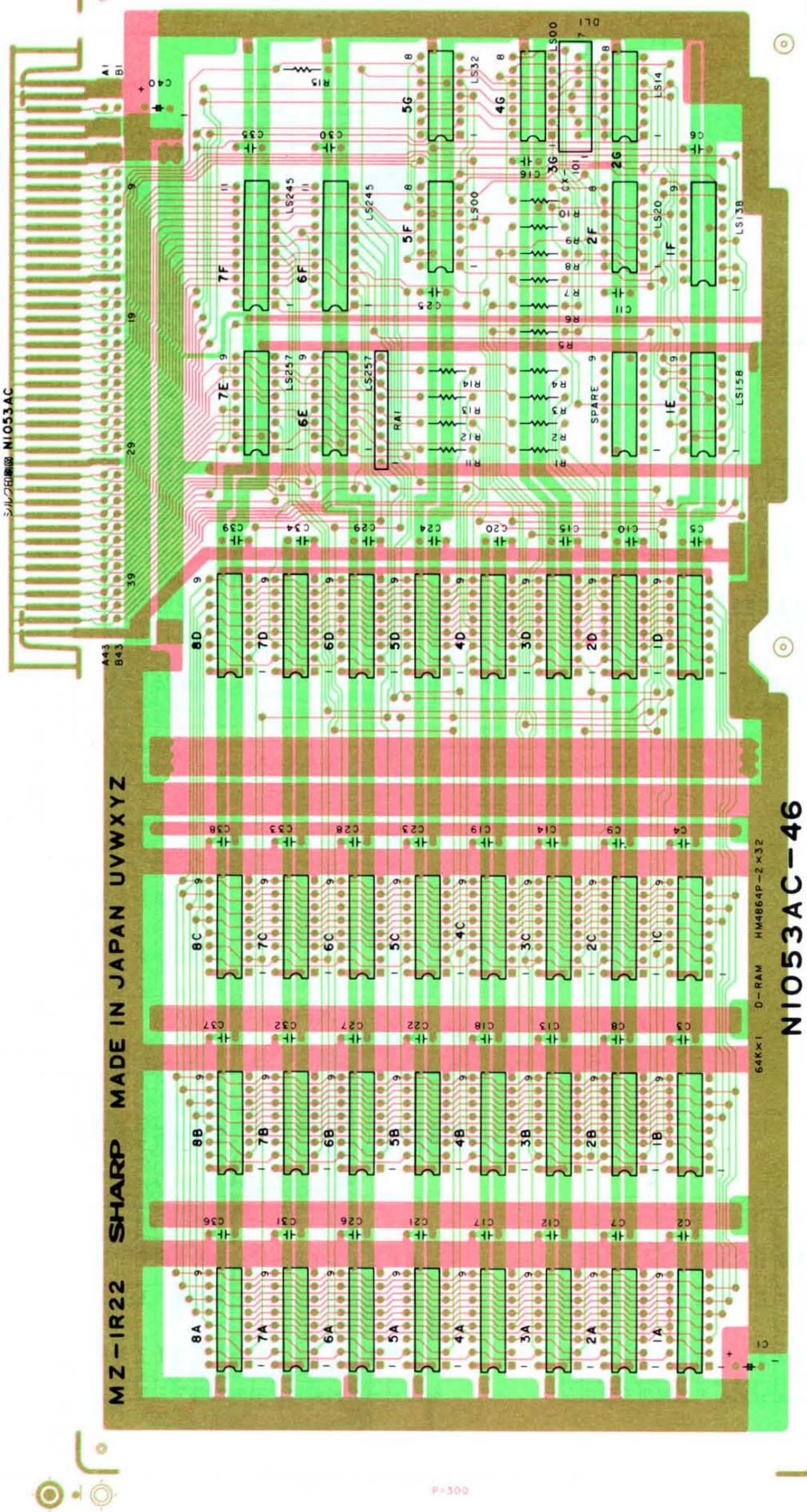


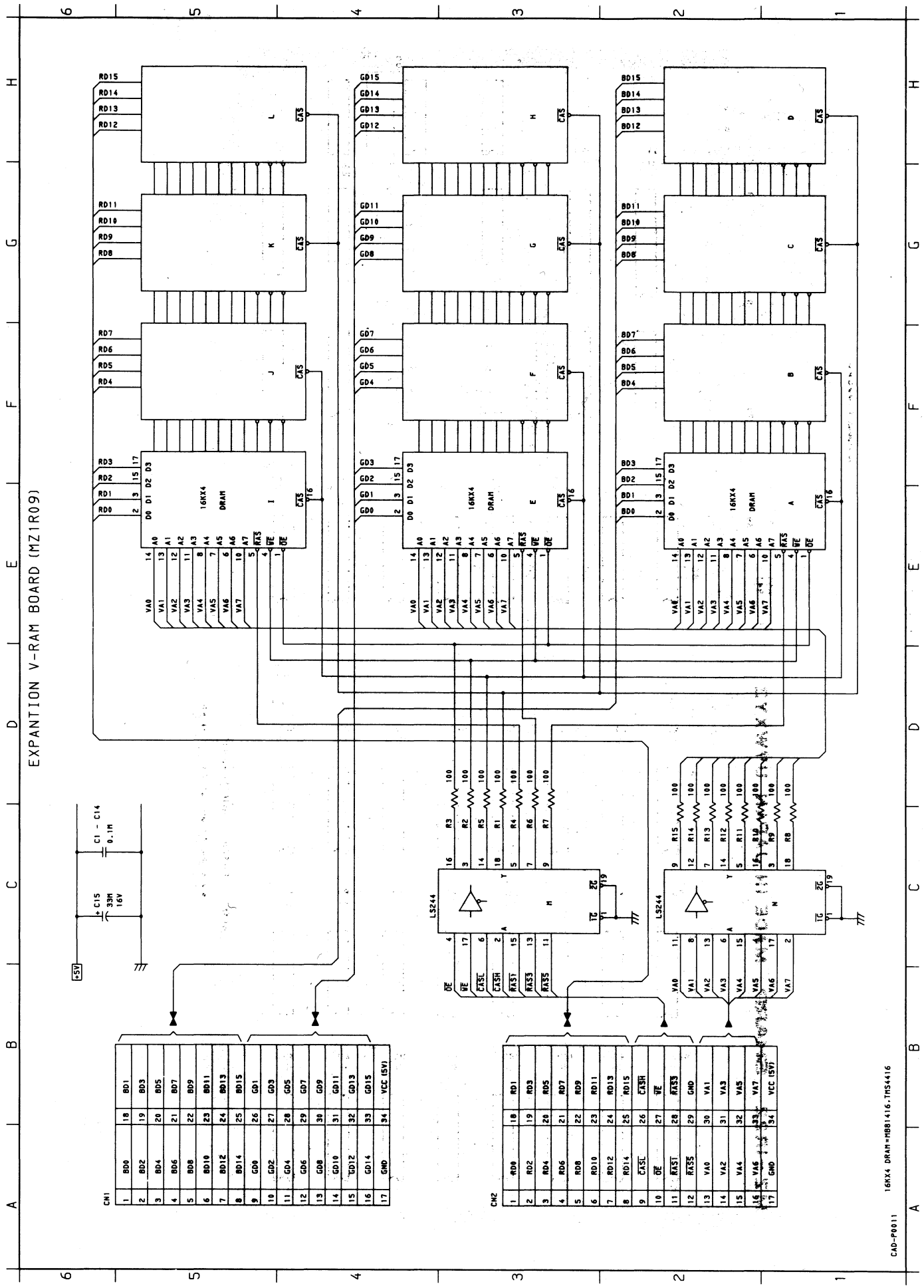
MZ1R11 D-RAM BOARD LAYOUT



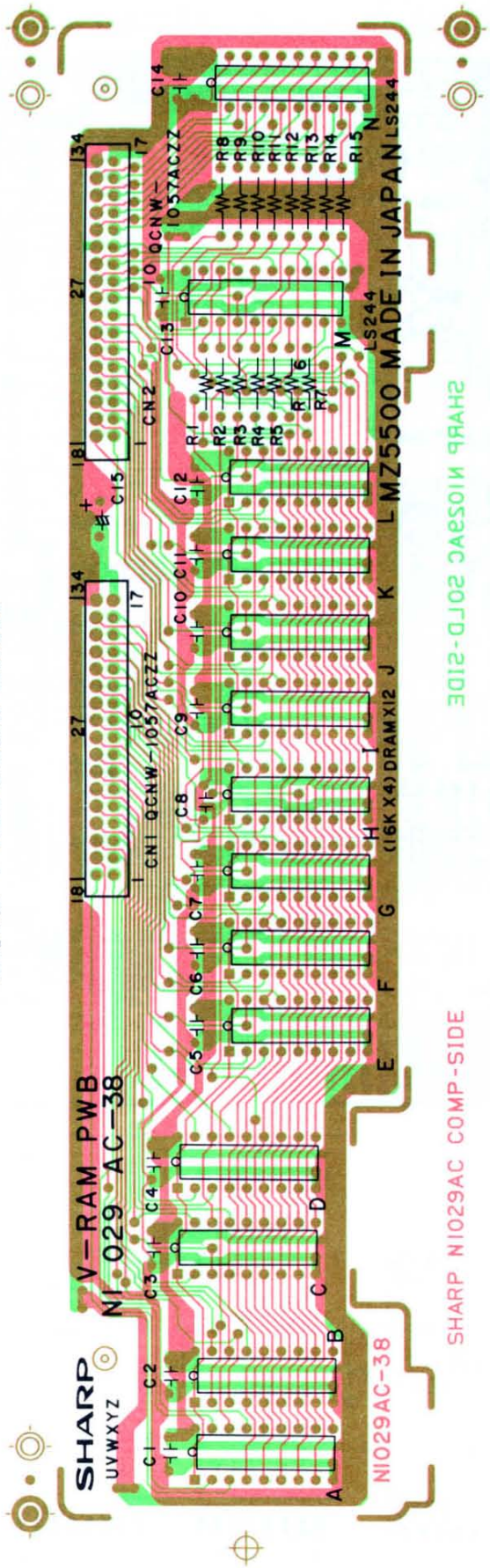


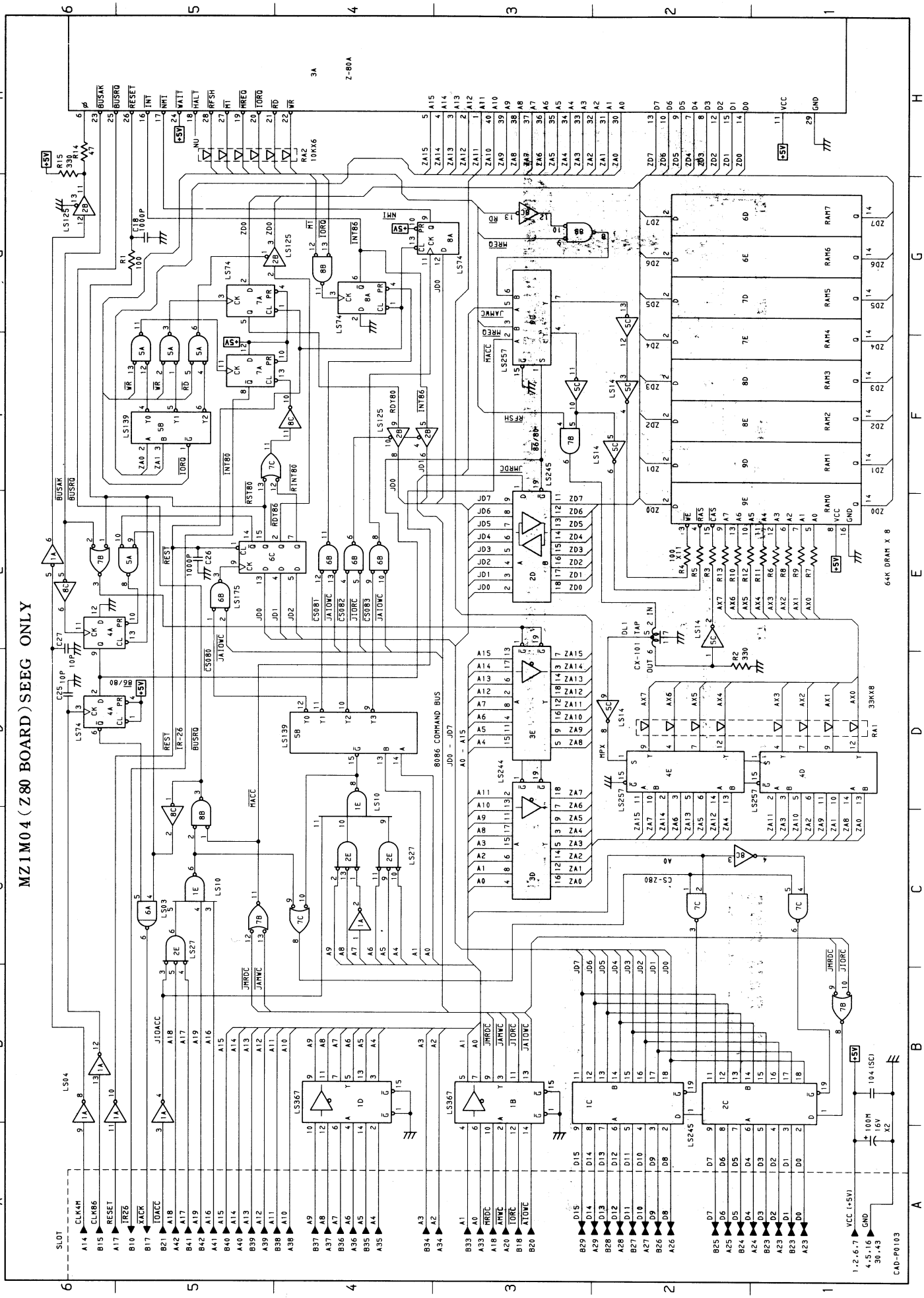
MZ1R22 D-RAM BOARD LAYOUT



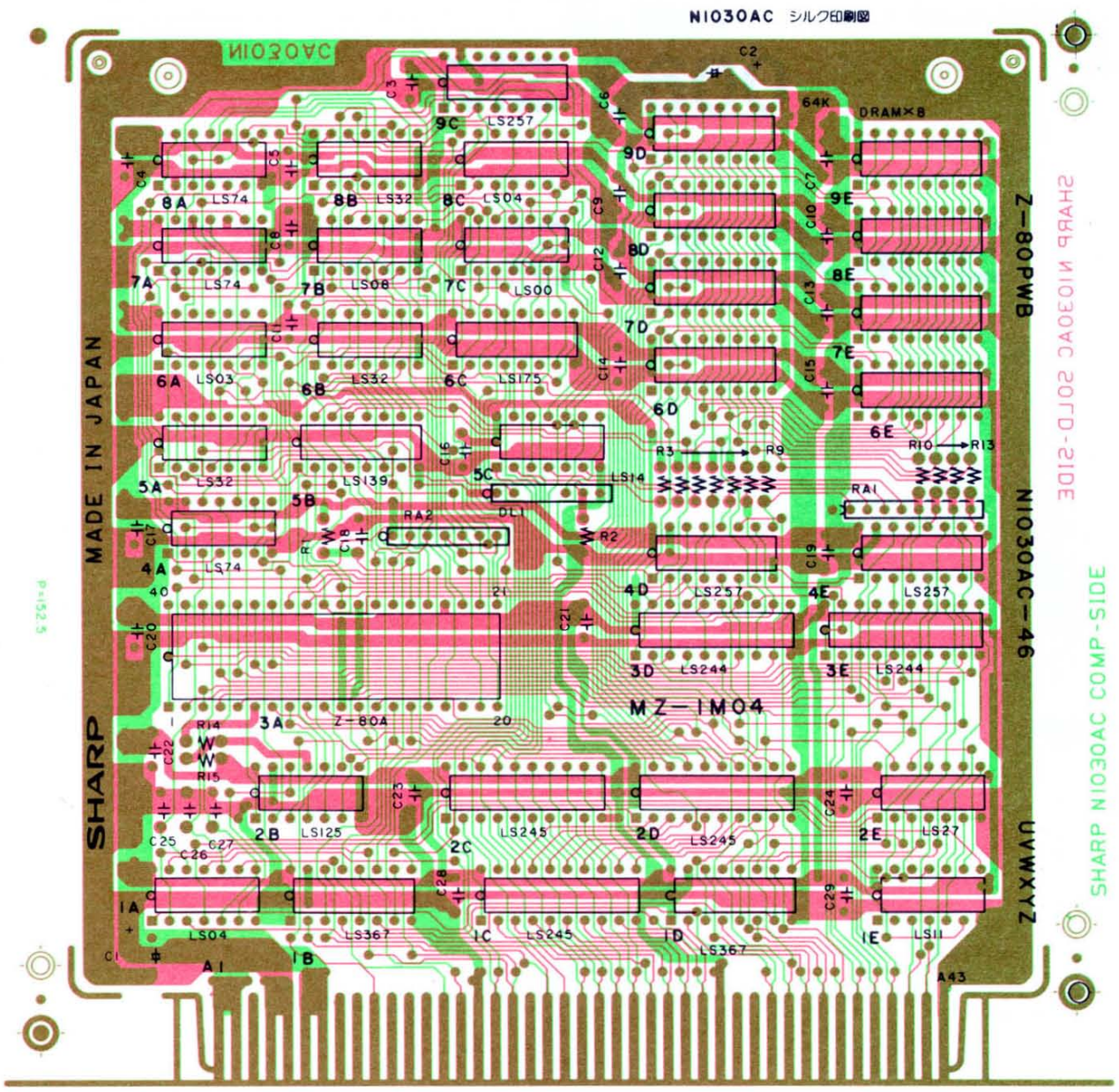


MZ1R09 V-RAM BOARD LAYOUT





MZ1M04(Z80 BOARD)SEEG ONLY



MZ-5600

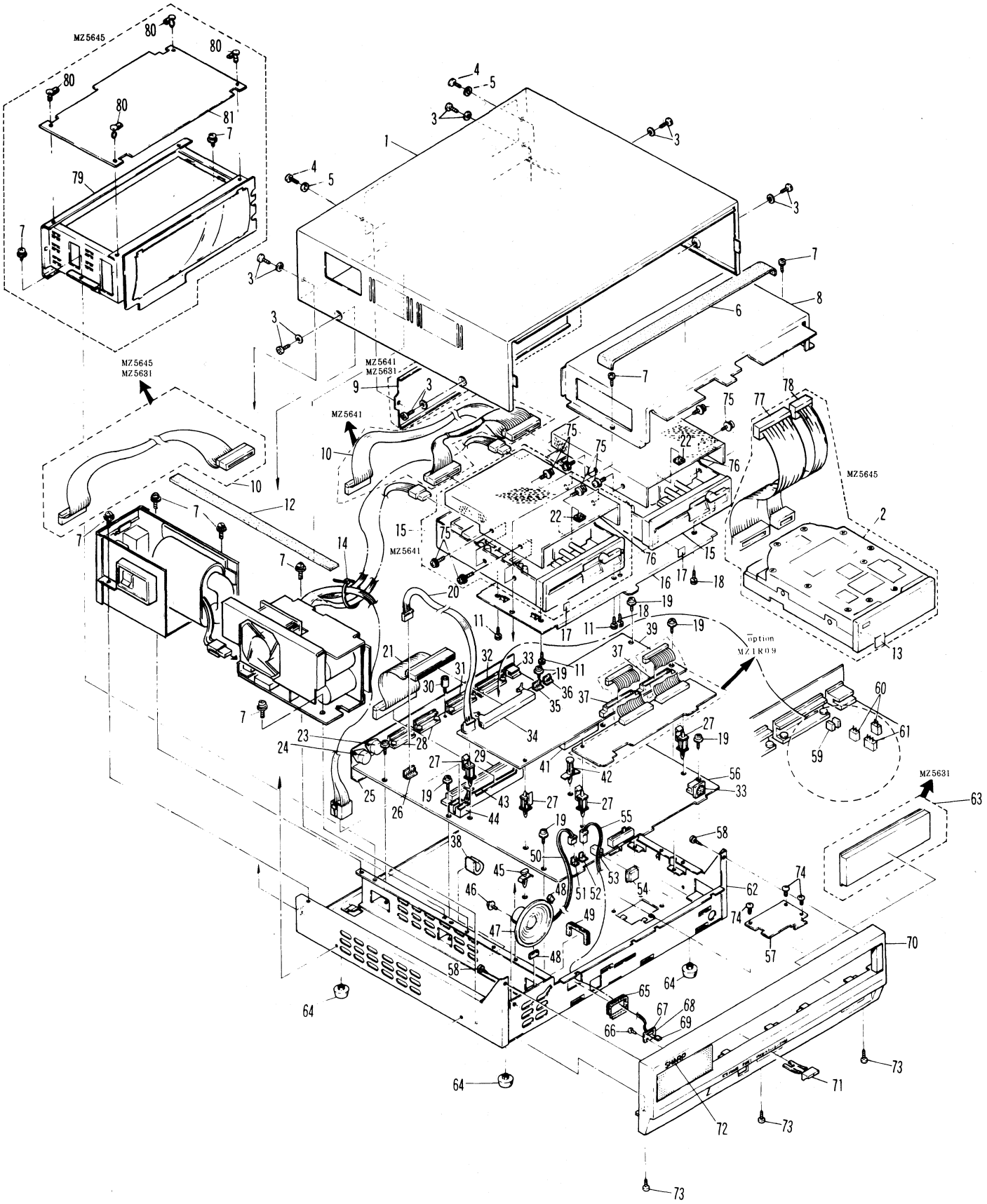
PARTS LIST & GUIDE

1 Exteries

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	CCABA1015ACZB	BC		D	Top cabinet
2	DUNTK1318ACZZ	**	N	C	Hard disk drive unit (MZ5645)
3	LX-BZ0038FCZZ	AA		C	Screw
4	XBBSC30P080000	AA		C	Screw (3×8)
5	XWHNZ30-05080	AA		C	Washer
6	PCUSS1008ACZZ	AD		C	Cushion
7	XBPSD40P08K00	AA		C	Screw (4×8K)
8	LANGF1069ACZZ	AP		C	Sub angle
9	HPNLC1002ACZA	AL	N	D	Panel (MZ5641,MZ5631)
10	QCNW-1053ACZZ	AV		C	Lead wire (PS~FD) (MZ5645,MZ5631)
	QCNW-1056ACZZ	AZ		C	Lead wire (PS~FD) (MZ5641)
11	XBPSD40P05K00	AA		C	Screw (4×5K) (MZ5645)
	XBPSD30P08K00	AA		C	Screw (3×8K) (MZ5641)
12	PCUSS1011ACZZ	AE	N	C	Cushion
13	TLABZ1050ACZA	AB		C	Drive label (MZ5645)
14	LBNDJ0004UCZZ	AA		C	Cable band
15	DUNT-1357ACZZ	**		E	MFD unit
16	LANGT1070ACZZ	AL		C	MFD plate
17	TLABZ1035ACZA	AB		C	Drive label
18	XBPSD30P08K00	AA		C	Screw (3×8K)
19	XBPSD30P06KS0	AA		C	Screw (3×6KS)
20	QCNW-1055ACZZ	AG		C	Lead wire (CPU~CRT)
21	QCNW-1054ACZZ	AW		C	Lead wire (CPU~CRT)
22	PCUSS1002ACZZ	AA		C	Speaker cushion
23	QCNCW1045ACZZ	AP		C	Connector (5pin)
24	QCNCW1040ACZZ	AR		C	Din connector for colour moniter
25	LANGT1043ACZZ	AL		C	CPU PWB angle
26	QCNCM1009ACZH	AC		C	Connector (8pin)
27	LSUPP1003ACZZ	AB		C	Spacer
28	QCNCW1021ACZZ	AS		C	Connector (15pin)
29	QCNCW1023ACZZ	AT		C	Connector (86pin)
30	LX-BZ1001ACZZ	AC		C	Screw
31	QCNCW1022ACZZ	AU		C	Connector (25pin)
32	QCNCW1029ACZZ	AU		C	Connector (25pin)
33	QCNCW1017ACZZ	AF		C	Connector (8pin)
34	QCNCM1027ACZZ	AP		C	Connector (60pin)
35	QCNCM1009ACZE	AB		C	Connector (5pin)
36	QCNCM1009ACZD	AB		C	Connector (4pin)
37	QCNCM1026ACZZ	AK		C	Connector (34pin)
38	LHLDW2334RCZZ	AC		C	Wire holder (MZ5631)
39	DUNT-1182ACZZ	**		E	CRT PWB unit (Ref. block [2])
41	QCNCM1025ACZZ	AK		C	Connector (34pin)
42	LSUPP1002ACZZ	AC		C	Spacer
43	QCNCM1024ACZZ	AP		C	Connector (60pin)
44	QCNCW0207HCZZ	AK		C	Connector (8pin)
45	LSUPP1001ACZZ	AB		C	Spacer
46	XBPSD40P10KS0	AA		C	Screw (4×10KS)
47	VSP0080P-608N	AN		B	Speaker (P008P)
48	PCUSG1006ACZZ	AB		C	Rubber cushion
49	PHOG-1001ACZZ	AC		C	Rubber cushion
50	QCNCW1008AC05	AB		B	Connector (2pin with wires)
51	QCNCM1009ACZB	AA		B	Connector (2pin)
52	QCNCM1244CC0B	AC		B	Connector (2pin)
53	QJAKC1001ACZZ	AD		C	Pin jack
54	JBTN-1001ACZA	AB		C	Switch knob
55	QCNW-1025AC01	AC		C	Lead wire (LED~CPU)
56	DUNTK1392ACZZ	**		E	CPU PWB unit (Ref. block [3])
57	GFTAU1023ACZZ	AM		C	ROM cover
58	XCPSD40P120000	AA		C	Screw (4×12)
59	QCNCW1035ACZZ	AC		B	Connector (2pin)
60	QCNCM1047ACZZ	AD		B	Connector (2pin)
61	QCNCM1048ACZZ	AE		B	Connector (3pin)
62	CCABA1018ACZA	BC	N	D	Bottom cabinet (This includes No 64)
63	GFTAF1018ACZA	AE		D	Cover (MZ5631)
64	GLEGP1005ACZZ	AB		C	Rubber foot
65	PHOG-1005ACZZ	AC		C	Protector rubber
66	XUPSD30P060000	AA		C	Screw (3×6)
67	VRD-ST2EY121J	AA		C	Resistor (1/4W 120Ω ±5%)
68	QPWBE1019ACZZ	AB		C	LED PWB (W/O parts)
69	VHPGL9PG2//-1	AC		B	LED (GL9PG2)
70	CCABC1014ACZB	AX		D	Operation panel (This includes No 71,72)
71	JKNBP1006ACZA	AD		C	Volume knob
72	HBDGB1002ACZZ	AD		C	"SHARP" Badge
73	XBTSC40P060000	AA		C	Screw (4×6)
74	XBPSD30P050000	AA		C	Screw (3×5)
75	XBSSD30P060000	AA		C	Screw (3×6)
76	PSLDM1005ACZZ	AN		C	Shield plate
77	QCNW-1098ACZZ	AS		C	HD cable (A) (MZ5645)
78	QCNW-1099ACZZ	AV		C	HD cable (B) (MZ5645)
79	DUNT-1341ACZZ	BU		E	Expantion unit (Ref. block [8]) (MZ5645) Except Europe

1 Exteries

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
79	DUNT-1377ACZZ	BU		E	Expantion unit (Ref. block 9)	(MZ5645) Europe only
80	LBNDJ0009FCZZ	AC		D	Clamp band	(MZ5645)
81	DUNTK1270ACZZ	**		E	H/D I/F PWB unit	(MZ5645)



2 CRT PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCM1009ACZD	AB		C	Connector (4pin)
2	QCNCM1009ACZE	AB		C	Connector (5pin)
3	QCNCM1026ACZZ	AK		C	Connector (34pin)
4	QCNCM1027ACZZ	AP		C	Connector (60pin)
5	QCNW-1055ACZZ	AG		C	Lead wire (CPU~CRT)
6	QPiN-0019MCZZ	AA		C	Pin (0Ω)
7	RCRS-1008ACZZ	AT		B	Crystal (28.64MHz)
8	RCRS-1009ACZZ	AT		B	Crystal (42.95MHz)
9	RMPTC8334QCKJ	AC		B	Block resistor (330KΩ×8 1/16W ±10%)
10	VCCCPU1HH200J	AB		C	Capacitor (50WV 20pF)
11	VCCCPU1HH300J	AA		C	Capacitor (50WV 30pF)
12	VCEAAU1CW107Q	AC		C	Capacitor (16WV 100μF)
13	VCKYPU1HB101K	AA		C	Capacitor (50WV 100pF)
14	VCKYPU1HB102K	AA		C	Capacitor (50WV 1000pF)
15	VCKYPU1HB221K	AB		C	Capacitor (50WV 220pF)
16	VCTYPU1NX104M	AB		C	Capacitor (12WV 0.10μF)
17	VHiHM6148P/-6	AV		B	IC (HM6148P)
18	VHiLZ90E07/-1	BP	N	B	IC (LZ90E07)
19	VHiM74LS00/-1	AE		B	IC (M74LS00P)
20	VHiM74LS04/-1	AE		B	IC (M74LS04P)
21	VHiM74LS08/-1	AE		B	IC (M74LS08)
22	VHiM74LS125-1	AH		B	IC (M74LS125P)
23	VHiM74LS138-1	AK		B	IC (M74LS138P)
24	VHiM74LS158-1	AG		B	IC (M74LS158P)
25	VHiM74LS244-1	AM		B	IC (M74LS244P)
26	VHiM74LS245-1	AM		B	IC (M74LS245P)
27	VHiM74LS32/-1	AF		B	IC (M74LS32P)
28	VHiM74LS374-1	AM		B	IC (M74LS374P)
29	VHiM74LS51/-1	AE		B	IC (M74LS51)
30	VHiM74LS670-1	AL		B	IC (M74LS670P)
31	VHiM74LS74/-1	AG		B	IC (M74LS74P)
32	VHiM74LS75/-1	AE		B	IC (M74LS75P)
33	VHiSN74LS122N	AH		B	IC (SN74LS122N)
34	VHiSN74LS166N	AN		B	IC (74LS166)
35	VHiSN74LS257N	AG		B	IC (SN74LS257N)
36	VHiSN74S74N-1	AF		B	IC (SN74S74N)
37	VHiSN7400N/-1	AG		B	IC (SN7400)
38	VHiSN7404N/-1	AF		B	IC (SN7404N)
39	VHiSP6102C034	BA	N	B	IC (SP6102C034)
40	VHiSP6102C035	BA	N	B	IC (SP6102C035)
41	VHiTMS4416-15	AZ	N	B	IC (TMS4416)
42	VHiUPD7220D-1	BS		B	LSI (UPD7220D)
44	VRD-ST2EY101J	AA		C	Resistor (1/4W 100Ω ±5%)
45	VRD-ST2EY103J	AA		C	Resistor (1/4W 10KΩ ±5%)
46	VRD-ST2EY220J	AA		C	Resistor (1/4W 22Ω ±5%)
47	VRD-ST2EY334J	AA		C	Resistor (1/4W 330KΩ ±5%)
48	VRD-SU2EY101J	AA		C	Resistor (1/4W 100Ω ±5%)
49	VRD-SU2EY331J	AA		C	Resistor (1/4W 330Ω ±5%)
	(Unit)				
901	DUNT-1182ACZZ	**		E	CRT PWB unit (Ref. block 1-39)

3 CPU PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	LANGT1043ACZZ	AL		C	CPU PWB angle
2	QCNCW0207HCZZ	AK		C	Connector (8pin)
3	QCNCM1009ACZB	AA		B	Connector (2pin)
4	QCNCM1009ACZH	AC		C	Connector (8pin)
5	QCNCM1009ACZJ	AC		C	Connector (10pin)
6	QCNCW1017ACZZ	AF		C	Connector (8pin)
7	QCNCW1021ACZZ	AS		C	Connector (15pin)
8	QCNCW1022ACZZ	AU		C	Connector (25pin)
9	QCNCW1023ACZZ	AT		C	Connector (86pin)
10	QCNCM1024ACZZ	AP		C	Connector (60pin)
11	QCNCM1025ACZZ	AK		C	Connector (34pin)
12	QCNCW1029ACZZ	AU		C	Connector (25pin)
13	QCNCW1035ACZZ	AC		B	Connector (2pin)
14	QCNCW1040ACZZ	AR		C	Din connector for colour moniter
15	QCNCW1045ACZZ	AP		C	Connector (5pin)
16	QCNCM1047ACZZ	AD		B	Connector (2pin)
17	QCNCM1048ACZZ	AE		B	Connector (3pin)
18	QCNCM1244CC0B	AC		B	Connector (2pin)
19	QJAKC1001ACZZ	AD		C	Pin jack
20	QSOCZ6418ACZZ	AD		C	IC socket (18pin)
21	QSOCZ6420ACZZ	AE		C	IC socket (20pin)
22	QSOCZ6428ACZZ	AE		C	IC socket (28pin)

3 CPU PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
23	QSOCZ6440ACZZ	AG		C	IC socket (40pin)
24	QSW-P1022ACZZ	AF		B	Push switch
25	QSW-Z2002SCZZ	AT		B	Dip switch
26	RC-KZ1018CCZZ	AE		C	Capacitor (250WV 25pF)
27	RC-KZ1026CCZZ	AF		C	Capacitor (40pF)
28	RCiLL1001ACZZ	AC		C	Coil
29	RCRSP1003CCZZ	AT		B	Crystal (32KHz)
30	RCRSQ1010ACZZ	AK		B	Crystal (14.7456MHz)
31	RCRS-1016ACZZ	AU		B	Crystal (24MHz)
32	RMPTC4102QCKJ	AC		B	Block resistor (1.0KΩ×4 1/16W ±10%)
33	RMPTC6331QCKB	AC		B	Block resistor (330Ω×6 1/8W ±10%)
34	RMPTC8224QCMJ	AD		B	Block resistor (220KΩ×8 1/16W ±20%)
35	RMPTC8682QCKJ	AD		B	Block resistor (6.8KΩ×8 1/16W ±10%)
36	RVR-Q1001ACZZ	AF		B	Variable resistor (50KΩ A type slide)
37	RVR-M1411QCZZ	AM		B	Veristor resistor (10KΩ)
38	RVR-M2411QCZZ	AP		B	Variable resistor (20KΩ)
39	UBATN1001ACZZ	AS		A	Battery
40	VCCCPU1HH120J	AA		C	Capacitor (50WV 12pF)
41	VCCCPU1HH470J	AA		C	Capacitor (50WV 47pF)
42	VCCCPU1HH510J	AB		C	Capacitor (50WV 51pF)
43	VCCCPU1HH560J	AA		C	Capacitor (50WV 56pF)
44	VCCCPU1HH820J	AB		C	Capacitor (50WV 82pF)
45	VCEAAU1CW106Q	AB		C	Capacitor (16WV 10μF)
46	VCEAAU1CW107Q	AC		C	Capacitor (16WV 100μF)
47	VCEAAU1CW226Q	AB		C	Capacitor (16WV 22μF)
48	VCEAAU1CW227Q	AC		C	Capacitor (16WV 220μF)
49	VCEAAU1CW336Q	AB		C	Capacitor (16WV 33μF)
50	VCEAAU1EW227Q	AD		C	Capacitor (25WV 220μF)
51	VCEAAU1EW336Q	AB		C	Capacitor (25WV 33μF)
52	VCEAAU1HW225Q	AB		C	Capacitor (50WV 2.2μF)
53	VCEAAU1HW105Q	AB		C	Capacitor (50WV 1.0μF)
54	VCEAAU1HW335Q	AB		C	Capacitor (50WV 3.3μF)
55	VCKYPU1HB101K	AA		C	Capacitor (50WV 100pF)
56	VCKYPU1HB102K	AA		C	Capacitor (50WV 1000pF)
57	VCKYPU1HB121K	AA		C	Capacitor (50WV 120PF)
58	VCKYPU1HB221K	AB		C	Capacitor (50WV 220pF)
59	VCKYPU1HB222K	AA		C	Capacitor (50WV 2200pF)
60	VCKYPU1HB561K	AA		C	Capacitor (50WV 560pF)
61	VCKYPU1HB681K	AA		C	Capacitor (50WV 680PF)
62	VCKYPU1HB682K	AA		C	Capacitor (50WV 6800pF)
63	VCQSTT2TS271J	AD		C	Capacitor (150WV 270PF)
64	VCQYKU1HM102K	AA		C	Capacitor (50WV 0.001μF)
65	VCQYKU1HM152K	AA		C	Capacitor (50WV 1500pF)
66	VCQYKU1HM333K	AB		C	Capacitor (50WV 0.033μF)
67	VCQYKU1HM472K	AA		C	Capacitor (50WV 4700pF)
68	VCQYKU1HM682K	AB		C	Capacitor (50WV 6800pF)
69	VCTYPU1NX104M	AB		C	Capacitor (12WV 0.10μF)
70	VHDDS1588L2-1	AB		B	Diode (DS1588L2)
71	VHiAY38912/-1	AY		B	IC (AY38912)
72	VHiCX101///-1	AU		B	IC (CX101)
73	VHiHA16632AP1	BH		B	IC (HA16632)
74	VHiHM6148HL45	AV		B	IC (HM6148HL45)
75	VHiLH0082A/-1	AR		B	IC (LH0082A)
76	VHiLH0084A/-1	AW		B	IC (LH0084A)
77	VHiM74LS00/-1	AE		B	IC (M74LS00P)
78	VHiM74LS02/-1	AE		B	IC (M74LS02P)
79	VHiM74LS04/-1	AE		B	IC (M74LS04P)
80	VHiM74LS08/-1	AE		B	IC (M74LS08)
81	VHiM74LS10/-1	AE		B	IC (M74LS10P)
82	VHiM74LS11/-1	AE		B	IC (M74LS11P)
83	VHiM74LS123-1	AG		B	IC (M74LS123)
84	VHiM74LS125-1	AH		B	IC (M74LS125P)
85	VHiM74LS132-1	AH		B	IC (M74LS132P)
86	VHiM74LS138-1	AK		B	IC (M74LS138P)
87	VHiM74LS139-1	AL		B	IC (M74LS139P)
88	VHiM74LS14/-1	AM		B	IC (M74LS14P)
89	VHiM74LS151-1	AK		B	IC (M74LS151)
90	VHiM74LS157-1	AK		B	IC (M74LS157P)
91	VHiM74LS158-1	AG		B	IC (M74LS158P)
92	VHiM74LS163-1	AH		B	IC (M74LS163P)
93	VHiM74LS164-1	AH		B	IC (M74LS164P)
94	VHiM74LS173-1	AG		B	IC (M74LS173P)
95	VHiM74LS174-1	AK		B	IC (M74LS174P)
96	VHiM74LS175-1	AG		B	IC (M74LS175P)
97	VHiM74LS20/-1	AE		B	IC (M74LS20P)
98	VHiSN74LS21-1	AE		B	IC (SN74LS21N)
99	VHiM74LS245-1	AM		B	IC (M74LS245P)
100	VHiM74LS257-1	AQ		B	IC (M74LS257P)
101	VHiM74LS27/-1	AF		B	IC (M74LS27)
102	VHiM74LS30/-1	AE		B	IC (M74LS30P)

3 CPU PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
103	VHiM74LS32/-1	AF		B	IC (M74LS32P)
104	VHiM74LS365-1	AF		B	IC (M74LS365P)
105	VHiM74LS367-1	AH		B	IC (M74LS367P)
106	VHiM74LS373-1	AM		B	IC (M74LS373P)
107	VHiM74LS393-1	AN		B	IC (M74LS393P)
108	VHiM74LS74/-1	AG		B	IC (M74LS74P)
109	VHiM74LS86/-1	AF		B	IC (M74LS86P)
110	VHiNE555///-1	AG		B	IC (NE555)
111	VHiRP5C01//-1	AV		B	IC (RP5C01)
112	VHiSN74LS00-1	AE		B	IC (SN74LS00N)
113	VHiSN74LS541N	AP		B	IC (SN74LS541N)
114	VHiSN7404N/-1	AF		B	IC (SN7404N)
115	VHiSN7406N/-1	AG		B	IC (SN7406N)
116	VHiSN7438N/-1	AF		B	IC (HD7438P)
117	VHiSN75188N-1	AM		B	IC (SN75188N)
118	VHiSN75189A-1	AP		B	IC (SN75189AN)
119	VHiTA7313AP-1	AL		B	IC (TA7313AP)
120	VHiUPD765//-1	BK		B	IC (UPD765)
121	VHiUPD8255/-1	AV		B	LSI (UPD8255)
122	VHi2764//AC63	BK	N	B	IC (2764)
	VHi2764//AC64	BK	N	B	IC (2764)
123	VHi4164-150-H	AZ		B	IC (4164)
124	VHi8086////-2	BN		B	IC (8086)
125	VHi8237A-5M-N	BC		B	IC (8237A5MN)
126	VHi8259A///-1	AT		B	LSI (8259A)
127	VHi8284A///-1	AY		B	LSI (8284A)
128	VHi8288////-1	BG		B	LSI (8288)
129	VCTYPU1EX472F	AA		C	Capacitor (25WV 4700pF)
130	VRD-ST2EY101J	AA		C	Resistor (1/4W 100Ω ±5%)
131	VRD-ST2EY102J	AA		C	Resistor (1/4W 1KΩ ±5%)
132	VRD-ST2EY103J	AA		C	Resistor (1/4W 10KΩ ±5%)
133	VRD-ST2EY104J	AA		C	Resistor (1/4W 100KΩ ±5%)
134	VRD-ST2EY122J	AA		C	Resistor (1/4W 1.2KΩ ±5%)
135	VRD-ST2EY221J	AA		C	Resistor (1/4W 220Ω ±5%)
136	VRD-ST2EY223J	AA		C	Resistor (1/4W 22KΩ ±5%)
137	VRD-ST2EY331J	AA		C	Resistor (1/4W 330Ω ±5%)
138	VRD-ST2EY332J	AA		C	Resistor (1/4W 3.3KΩ ±5%)
139	VRD-ST2EY333J	AA		C	Resistor (1/4W 33KΩ ±5%)
140	VRD-ST2EY392J	AA		C	Resistor (1/4W 3.9KΩ ±5%)
141	VRD-ST2EY471J	AA		C	Resistor (1/4W 470Ω ±5%)
142	VRD-ST2EY472J	AA		C	Resistor (1/4W 4.7KΩ ±5%)
143	VRD-ST2EY473J	AA		C	Resistor (1/4W 47KΩ ±5%)
144	VRD-ST2EY561J	AA		C	Resistor (1/4W 560Ω ±5%)
145	VRD-ST2EY183J	AA		C	Resistor (1/4W 18KΩ ±5%)
146	VRD-ST2EY563J	AA		C	Resistor (1/4W 56KΩ ±5%)
147	VRD-ST2EY682J	AA		C	Resistor (1/4W 6.8KΩ ±5%)
148	VRD-SU2EY121J	AA		C	Resistor (1/4W 120Ω ±5%)
149	VRD-SU2EY152J	AA		C	Resistor (1/4W 1.5KΩ ±5%)
150	VRD-SU2EY224J	AA		C	Resistor (1/4W 220KΩ ±5%)
151	VRD-SU2EY241J	AA		C	Resistor (1/4W 240Ω ±5%)
152	VRD-SU2EY391J	AA		C	Resistor (1/4W 390Ω ±5%)
153	VRD-SU2EY470J	AA		C	Resistor (1/4W 47Ω ±5%)
154	VRD-SU2EY511J	AA		C	Resistor (1/4W 510Ω ±5%)
155	VRD-SU2EY560J	AA		C	Resistor (1/4W 56Ω ±5%)
156	VRD-SU2EY680J	AA		C	Resistor (1/4W 68Ω ±5%)
157	VRD-SU2EY681J	AA		C	Resistor (1/4W 680Ω ±5%)
158	VRD-SU2EY750J	AA		C	Resistor (1/4W 75Ω ±5%)
159	VRD-SU2EY821J	AA		C	Resistor (1/4W 820Ω ±5%)
160	VRD-SU2EY824J	AA		C	Resistor (1/4W 820KΩ ±5%)
161	VRD-ST2EY123J	AA		C	Resistor (1/4W 12KΩ ±5%)
162	VRN-RT2EK153F	AB		C	Resistor (1/4W 15KΩ ±1%)
163	VRN-RT2EK203F	AB		C	Resistor (1/4W 20KΩ ±1%)
164	VRN-RT2EK513F	AB		C	Resistor (1/4W 51KΩ ±1%)
165	VS2SA673-D/-1	AC		B	Transistor (2SA673)
166	VS2SA733-//-1	AD		B	Transistor (2SA733)
167	VS2SC1317-S-1	AC		B	Transistor (2SC1317)
168	VS2SC641KC/-1	AE		B	Transistor (2SC641KC)
169	VS2SC945///-1	AD		B	Transistor (2SC945)
170	VS2SK168-//-1	AD		B	FET (2SK168)
171	XBPSM30P04K00	AA		C	Screw (3×4K)
172	XBPSM30P10K00	AA		C	Screw (3×10K)
	(Unit)				
901	DUNTK1392ACZZ	**		E	CPU PWB unit (Ref. block 1-56)

4 Key PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCW1007ACZZ	AE	N	C	Connector (18pin)
2	QCNCM1009ACZi	AC		C	Connector (9pin)
3	QCNCW1018ACZZ	AF		C	Connector (5pin)
4	QCNCW1300CC1D	AD		C	Connector (14pin)
5	QSOCZ6440ACZZ	AG		C	IC socket (40pin)
6	RCRS−1004ACZZ	AG		B	Crystal (6MHZ)
7	RMPTC8333QCKJ	AD		B	Block risistor (33KΩ×8 1/16W ±10%)
8	VCCCPU1HH100D	AA		C	Capacitor (50WV 10pF)
9	VCEAAU1CW336Q	AB		C	Capacitor (16WV 33μF)
10	VCEAAU1EW475Q	AB		C	Capacitor (25WV 4.7μF)
11	VCKYPU1HB681K	AA		C	Capacitor (50WV 680pF)
12	VCTYPU1NX104M	AB		C	Capacitor (12WV 0.10μF)
13	VHDDS1588L2−1	AB		B	Diode (DS1588L2)
14	VHiM74LS05/−1	AE		B	IC (M74LS05)
15	VHiM74LS14/−1	AM		B	IC (M74LS14P)
16	VHiTC4514BP−1	AN		B	IC (TC4514BP)
17	VHi8749//AC31	BS	N	B	IC (8749)
18	VRD−ST2EY100J	AA		C	Resistor (1/4W 10Ω ±5%)
19	VRD−ST2EY101J	AA		C	Resistor (1/4W 100Ω ±5%)
20	VRD−ST2EY102J	AA		C	Resistor (1/4W 1KΩ ±5%)
21	VRD−ST2EY104J	AA		C	Resistor (1/4W 100KΩ ±5%)
22	VRD−ST2EY121J	AA		C	Resistor (1/4W 120Ω ±5%)
23	VRD−ST2EY222J	AA		C	Resistor (1/4W 2.2KΩ ±5%)
24	VRD−ST2EY333J	AA		C	Resistor (1/4W 33KΩ ±5%)
25	VRD−ST2EY472J	AA		C	Resistor (1/4W 4.7KΩ ±5%)
26	VRD−ST2EY681J	AA		C	Resistor (1/4W 680Ω ±5%)
27	VRD−ST2EY682J	AA		C	Resistor (1/4W 6.8KΩ ±5%)
28	VS2SC945///−1	AD		B	Transistor (2SC945)
	(Unit)				
901	DUNTK1384ACZZ	BV		E	Key PWB unit (MZ1K11) (English only) (Ref. block 5−11)
	DUNTK1395ACZZ	BV		E	Key PWB unit (MZ1K09,MZ1K10) (Except English) (Ref. block 5−11)

5 Keyboard unit (MZ1K09,MZ1K10,MZ1K11)

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	CCABB1012ACZA	AT	N	D	Top cabinet	(This includes No 2,3,5)
2	GCOVH1004ACZZ	AC		D	cover plate S	
3	GCOVH1003ACZZ	AD		D	cover plate B	
4	TLABZ1029ACZA	AB		C	Power label	
5	HBDGB1002ACZZ	AD		C	"SHARP" Badge	
6	QCNW-1052ACZZ	AY		C	Cable	
7	QCNCW1018ACZZ	AF		C	Connector (5pin)	
8	QCNCM1009ACZi	AC		C	Connector (9pin)	
9	QCNCW1300CC1D	AD		C	Connector (14pin)	
10	QCNCW1007ACZZ	AE	N	C	Connector (18pin)	
11	DUNTK1384ACZZ	BV		E	Key PWB unit (MZ1K11)	(English only) (Ref. block 4)
	DUNTK1395ACZZ	BV		E	Key PWB unit (MZ1K09,MZ1K10)	(Except English) (Ref. block 4)
12	XBPSM30P06KS0	AA		C	Screw (3×6KS)	
13	XUPSC30P100000	AA		C	Screw (3×10)	
14	GLEGP1001CCZZ	AB		C	Lubber foot	
15	GSTN-1015ACZA	AF	N	C	Stand	
16	CCABA1010ACZA	AU	N	D	Bottom cabinet	(This includes No14,15)
17	PSLDM1004ACZZ	AM		D	Shield plate	
101	00PKCL10903-Z	AH		B	Push switch	
102	00PKCL10901-Z	AH		B	Push switch	
103	00PKCL10004-Z	AH		B	Push switch	
104	00P08KC392A//	BK	N	C	Panel	(English only)
	00P08KC275B//	BK	N	C	Panel	(Except English)
105	00P16KC004A//	AG		C	Guide	
106	00P16KF006A//	AG		C	Guide pin	
107	00P19KC003A//	AE		C	Lever holder	
108	00P21KC013A//	AE		C	Lever	
109	00P21KC006A//	AN		C	Lever (2)	
110	00P21KC005A//	AK		C	Lever (1.75)	
111	00P21KC007A//	AN		C	Lever (8)	
112	00P24KC032A//	AN		C	Spacer	
113	00P24KC027A//	AK		C	Spacer	
115	00P4D07177A//	AK	N	B	Diode (GL-9PR2)	
116	00PKCL11902-Z	AL	N	B	Push switch	(English only)
	00PKCL11901-Z	AP	N	B	Push switch	(Except English)
117	XBPSD30P040000	AA		C	Screw (3×4)	
120	00P29KF006B//	AK		C	Lead wire	
121	00P29KC049A//	AK		C	Lead wire	
122	00P23KF001A//	AC		C	Sub plate	
123	00P25KF008A//	AC		C	Shield plate	
124	00P13KF015A//	AB		C	Terminal	
125	00P24KC015N//	AD		C	Spacer	
126	00P21KC008A//	AK	N	C	Lever (3)	(Except English)
150	VHD1S2075K/-1	AB		B	Diode (1S2075K)	
201	00PC5KC083001	AK	N	C	Key top	
202	00PC5KC083002	AK	N	C	Key top	
203	00PC5KC083003	AK	N	C	Key top	
204	00PC5KC083004	AK	N	C	Key top	
205	00PC5KC083005	AK	N	C	Key top	
206	00PC5KC083006	AK	N	C	Key top	
207	00PC5KC083007	AK	N	C	Key top	
208	00PC5KC083008	AK	N	C	Key top	
209	00PC5KC083009	AK	N	C	Key top	
210	00PC5KC083010	AK	N	C	Key top	
211	00PC5KC083011	AK	N	C	Key top	
212	00P84E1C41001	AQ	N	C	Key top	
213	00P86N1C52044	AK	N	C	Key top	(French only)
	00P86N1C52001	AK	N	C	Key top	(Except French)
214	00P86N1C52045	AK	N	C	Key top	(French only)
	00P86N1C52014	AK	N	C	Key top	(Except French)
215	00P86N1C52046	AK	N	C	Key top	(French)
	00P86N1C52023	AK	N	C	Key top	(Germany)
	00P86N1C52074	AK	N	C	Key top	(English)
216	00P86N1C52047	AK	N	C	Key top	(French only)
	00P86N1C52004	AK	N	C	Key top	(Except French)
217	00P86N1C52048	AK	N	C	Key top	(French only)
	00P86N1C52005	AK	N	C	Key top	(Except French)
218	00P86N1C52049	AK	N	C	Key top	(French only)
	00P86N1C52015	AK	N	C	Key top	(Except French)
219	00P86N1C52050	AK	N	C	Key top	(French)
	00P86N1C52024	AK	N	C	Key top	(Germany)
	00P86N1C52016	AK	N	C	Key top	(English)
220	00P86N1C52051	AK	N	C	Key top	(French only)
	00P86N1C52017	AK	N	C	Key top	(Except French)
221	00P86N1C52078	AK	N	C	Key top	(French only)
	00P86N1C52018	AK	N	C	Key top	(Except French)
222	00P86N1C52053	AK	N	C	Key top	(French)
	00P86N1C52025	AK	N	C	Key top	(Germany)
	00P86N1C52019	AK	N	C	Key top	(English)
223	00P86N1C52054	AK	N	C	Key top	(French)

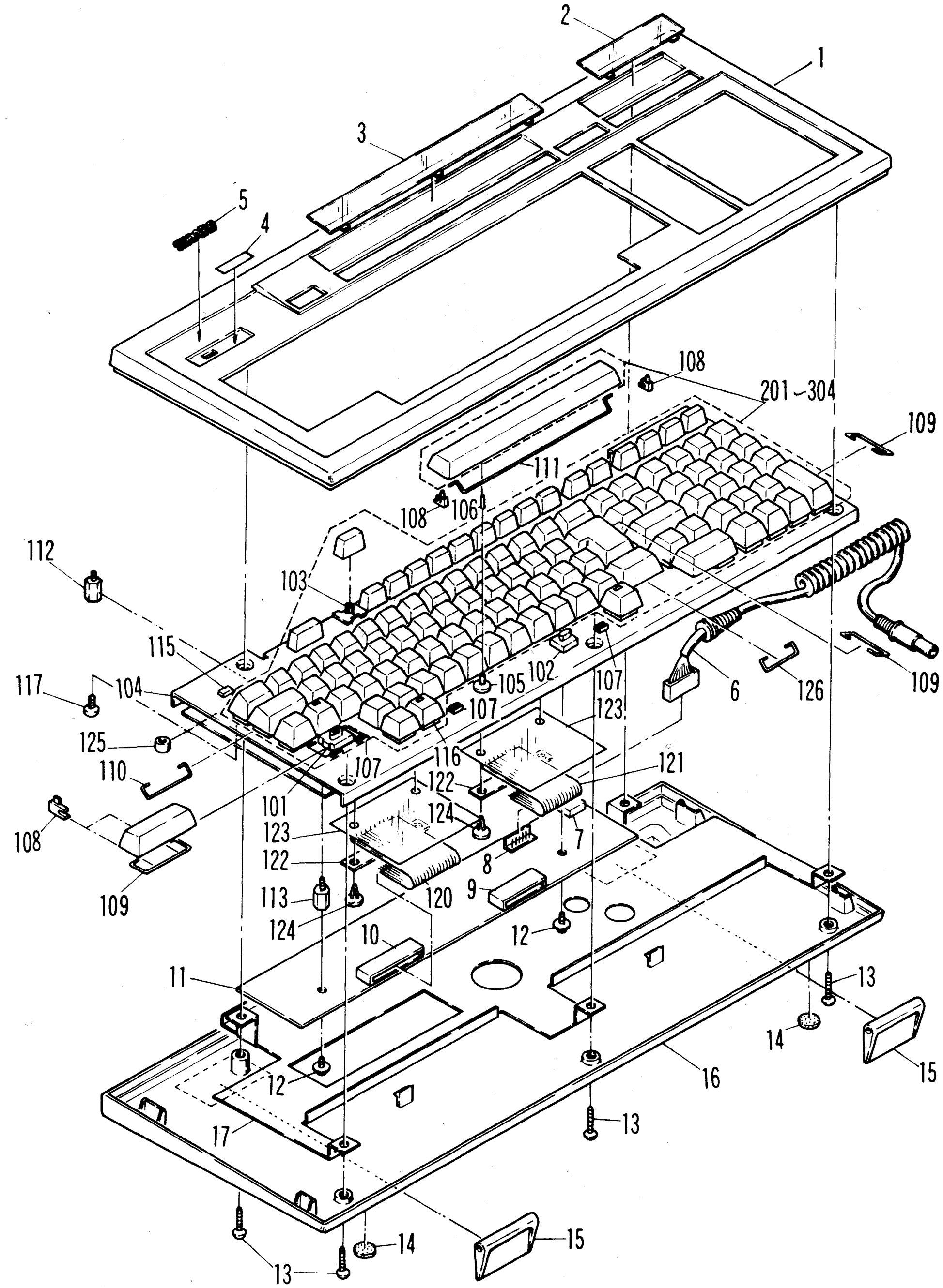
5 Keyboard unit (MZ1K09,MZ1K10,MZ1K11)

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
223	00P86N1C52026	AK	N	C	Key top	(Germany)
	00P86N1C52020	AK	N	C	Key top	(English)
224	00P86N1C52011	AK	N	C	Key top	(French)
	00P86N1C52027	AK	N	C	Key top	(Germany)
	00P86N1C52021	AK	N	C	Key top	(English)
225	00P86N4C52061	AK	N	C	Key top	(English only)
	00P86N1C52028	AK	N	C	Key top	(Except English)
226	00P81V3C41001	AQ	N	C	Key top	
227	00P82F5C41001	AQ	N	C	Key top	
228	00P86N2C52020	AK	N	C	Key top	(French only)
	00P86N2C52001	AK	N	C	Key top	(Except French)
229	00P86N2C52017	AK	N	C	Key top	(French only)
	00P86N2C52002	AK	N	C	Key top	(Except French)
230	00P86N2C52003	AK	N	C	Key top	
231	00P86N2C52004	AK	N	C	Key top	
232	00P86N2C52005	AK	N	C	Key top	
233	00P86N2C52017	AK	N	C	Key top	(Germany only)
	00P86N2C52006	AK	N	C	Key top	(Except Germany)
234	00P86N2C52007	AK	N	C	Key top	
235	00P86N2C52008	AK	N	C	Key top	
236	00P86N2C52009	AK	N	C	Key top	
237	00P86N2C52010	AK	N	C	Key top	
238	00P86N2C52026	AK	N	C	Key top	(French)
	00P86N2C52018	AK	N	C	Key top	(Germany)
	00P86N2C52016	AK	N	C	Key top	(English)
239	00P86N2C52027	AK	N	C	Key top	(French)
	00P86N2C52019	AK	N	C	Key top	(Germany)
	00P86N2C52011	AK	N	C	Key top	(English)
240	00P80M4C41001	AQ	N	C	Key top	
241	00P86N3C41096	AK	N	C	Key top	
242	00PD2KC0090001	AQ	N	C	Key top	
243	00P86N3C52021	AK	N	C	Key top	(French only)
	00P86N3C52001	AK	N	C	Key top	(Except French)
244	00P86N3C52002	AK	N	C	Key top	
245	00P86N3C52003	AK	N	C	Key top	
246	00P86N3C52004	AK	N	C	Key top	
247	00P86N3C52005	AK	N	C	Key top	
248	00P86N3C52006	AK	N	C	Key top	
249	00P86N3C52007	AK	N	C	Key top	
250	00P86N3C52008	AK	N	C	Key top	
251	00P86N3C52009	AK	N	C	Key top	
252	00P86N3C52022	AK	N	C	Key top	(French)
	00P86N3C52018	AK	N	C	Key top	(Germany)
	00P86N3C52015	AK	N	C	Key top	(English)
253	00P86N3C52048	AK	N	C	Key top	(French)
	00P86N3C52019	AK	N	C	Key top	(Germany)
	00P86N3C52016	AK	N	C	Key top	(English)
254	00P86N3C52047	AK	N	C	Key top	(French)
	00P86N3C52020	AK	N	C	Key top	(Germany)
	00P86N3C52017	AK	N	C	Key top	(English)
255	00P83L8C41001	AQ	N	C	Key top	
256	00P86N4C52001	AK	N	C	Key top	(English)
	00P86N4C52020	AK	N	C	Key top	(French)
	00P86N4C52015	AK	N	C	Key top	(Germany)
257	00P86N4C52002	AK	N	C	Key top	
258	00P86N4C52003	AK	N	C	Key top	
259	00P86N4C52004	AK	N	C	Key top	
260	00P86N4C52005	AK	N	C	Key top	
261	00P86N4C52006	AK	N	C	Key top	
262	00P86N4C52041	AK	N	C	Key top	(French only)
	00P86N4C52007	AK	N	C	Key top	(Except French)
263	00P86N4C52008	AK	N	C	Key top	(English)
	00P86N4C52042	AK	N	C	Key top	(French)
	00P86N4C52016	AK	N	C	Key top	(Germany)
264	00P86N4C52009	AK	N	C	Key top	(English)
	00P86N4C52043	AK	N	C	Key top	(French)
	00P86N4C52017	AK	N	C	Key top	(Germany)
265	00P86N4C52010	AK	N	C	Key top	(English)
	00P86N4C52044	AK	N	C	Key top	(French)
	00P86N4C52018	AK	N	C	Key top	(Germany)
266	00P86N4C52014	AK	N	C	Key top	(English only)
267	00P81T8C41002	AQ	N	C	Key top	(English only)
	00P80M2C41001	AQ	N	C	Key top	(Except English)
268	00P86N5C41001	AK	N	C	Key top	
269	00PD2KC0090002	AQ	N	C	Key top	
270	00P80L7C52000	AQ		C	Key top	
271	00PKB34884D//	AK	N	C	Key top	(English only)
	00P86N5C41002	AK	N	C	Key top	(Except English)
272	00PC5KC083012	AK	N	C	Key top	
273	00PC5KC083013	AK	N	C	Key top	

5 Keyboard unit (MZ1K09,MZ1K10,MZ1K11)

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
274	00P86N1C41001	AK	N	C	Key top
275	00P86N1C41002	AK	N	C	Key top
276	00P86N2C41001	AK	N	C	Key top
277	00P86N2C41002	AK	N	C	Key top
278	00P81T7C41001	AQ	N	C	Key top
279	00P86N4C41001	AK	N	C	Key top
280	00P86N4C41002	AK	N	C	Key top
281	00P81T9C41001	AQ	N	C	Key top
282	00P86P7C41000	AK	N	C	Key top (Half key blank)
283	00P86P7C41000	AK	N	C	Key top (Half key blank)
284	00P86P7C41000	AK	N	C	Key top (Half key blank)
285	00P86P7C41000	AK	N	C	Key top (Half key blank)
286	00P86N1C41003	AK	N	C	Key top
287	00P86N1C41004	AK	N	C	Key top
288	00P86N1C41005	AK	N	C	Key top
289	00P86N1C41006	AK	N	C	Key top
290	00P86N2C52013	AK	N	C	Key top
291	00P86N2C52014	AK	N	C	Key top
292	00P86N2C52015	AK	N	C	Key top
293	00P86N2C41003	AK	N	C	Key top
294	00P86N3C52013	AK	N	C	Key top
295	00P86P6C52001	AK	N	C	Key top
296	00P86N3C52014	AK	N	C	Key top
297	00P86N3C41097	AK	N	C	Key top
298	00P86N4C52011	AK	N	C	Key top
299	00P86N4C52012	AK	N	C	Key top
300	00P86N4C52013	AK	N	C	Key top
301	00P81U5C41001	AQ	N	C	Key top
302	00P86N5C52001	AK	N	C	Key top
303	00P86N5C52002	AK	N	C	Key top
304	00P86N5C52003	AK	N	C	Key top
400	TLABZ1031ACZZ	AE		C	Function Label (MZ1K11) (English only)
	TLABZ1040ACZZ	AE		C	Function label (MZ1K09,MZ1K10) (Except English)
401	TiNSE1175ACZZ	BS	N	D	Instruction book (MZ1K11) (English)
402	SPAKA1004ACZZ	AG	N	D	Packing cushion for Inst,Book
403	SPAKA1009ACZZ	AB		D	Packing sleeve for cable
404	SPAKA1413ACZZ	AD	N	D	Packing cushion
405	SPAKC1362ACZZ	AL	N	D	Packing case (for MZ1K09) (Germany)
	SPAKC1364ACZZ	AL	N	D	Packing case (for MZ1K10) (French)
	SPAKC1516ACZZ	AM	N	D	Packing case (for MZ1K11) (English)
406	SSAKA0001SCZZ	AA		D	Vinyl bag (200×300mm)
407	SSAKA3630QCZZ	AB		D	Vinyl bag (For key) (320×690mm)
	(Unit)				
901	QSW-K1025ACZZ	BR	N	E	Keyboard switch unit(MZ1K09) (Germany) (No 101~126,201~304)
	QSW-K1026ACZZ	BR	N	E	Keyboard switch unit(MZ1K10) (French) (No 101~126,201~304)
	QSW-K1029ACZZ	BR	N	E	Keyboard switch unit(MZ1K11) (English) (No 101~126,201~304)

5 Keyboard unit (MZ1K09,MZ1K10,MZ1K11)



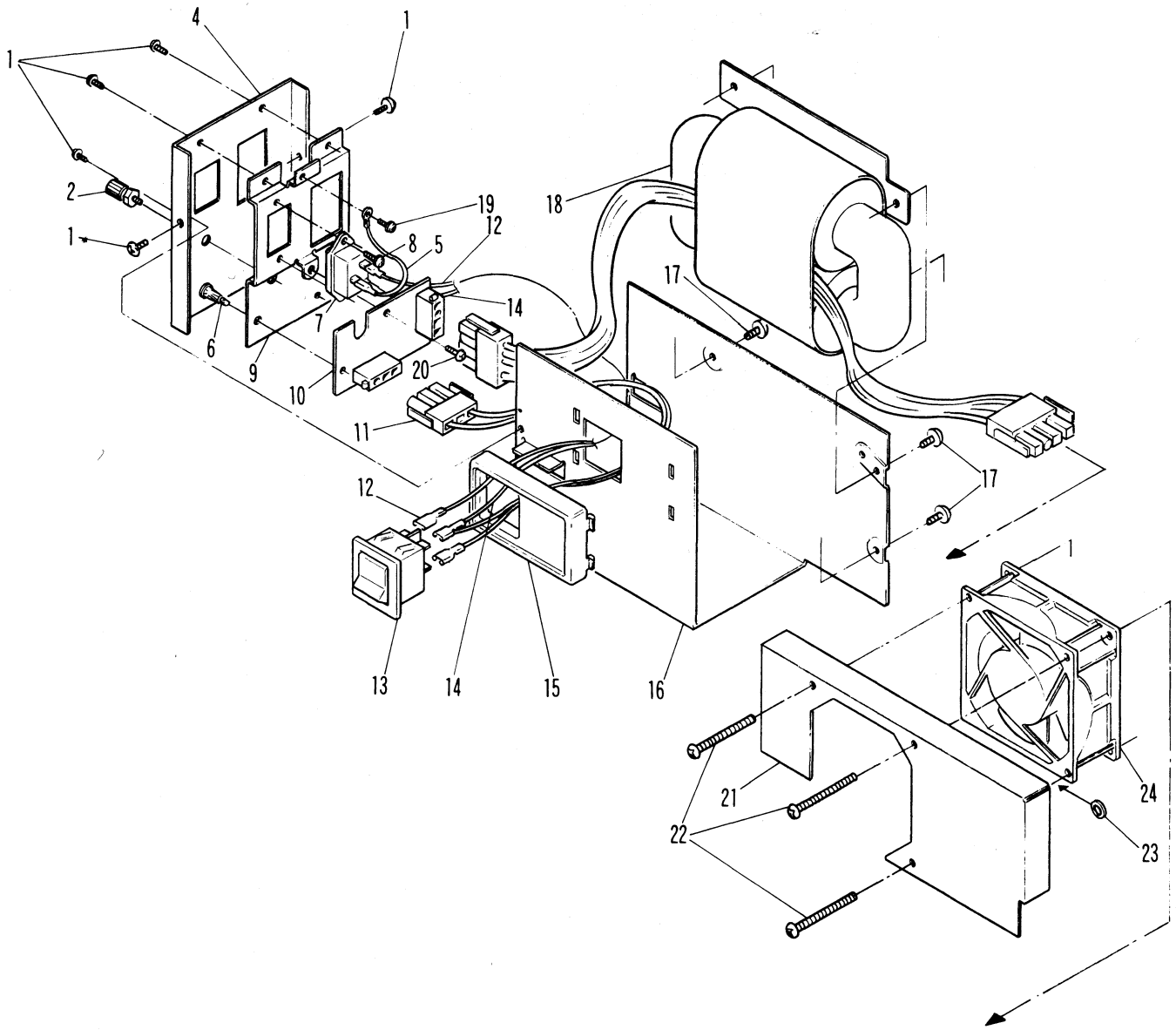
Keytop layout

201 · 202 203 204 205 206 207 208 209 210 211	272 273	282 283 284 285
212 213 214 215 216 217 218 219 220 221 222 223 224 226	274 275	286 287 288 289
227 228 229 230 231 232 233 234 235 236 237 238 239 240	276 277	290 291 292 293
241 242 243 244 245 246 247 248 249 250 251 252 253 254	278	294 295 296 297
255 225 256 257 258 259 260 261 262 263 264 265 266 267	279 280	298 299 300 301
268 269 270 271	281	302 303 304

※ Figure means refer number on the parts list.

6 Power supply (PR1.) unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	XBPSD30P05000	AA		C	Screw (3×5)
2	QTANN1004ACZZ	AE	N	C	Earth terminal
4	HPNLC1007ACZZ	AN		D	AC switch panel
5	QCNW-1082ACZZ	AC		C	Earth wire
6	PSPAN1007ACZZ	AB	N	C	Spacer
7	QSOCZ2027SCZZ	AK		C	AC socket (CM3)
8	XBBSD30P06000	AA		C	Screw (3×6)
9	LANGT1051ACZZ	AH		C	PWB angle
10	DUNTK1283ACZZ	AU		E	Power supply (PR1.) unit(200V) (No 100~105)
11	QCNW-1072ACZZ	AL		C	Lead wire
12	QCNW-1077ACZZ	AE		C	Lead wire (200V)
13	QSW-C9240QCZZ	AP		B	Seesaw switch
14	QCNW-1078ACZZ	AE		C	Lead wire (200V)
15	HPNLC1006ACZZ	AE		D	Switch panel
16	LCHSM1014ACZZ	AP		C	Power supply ind chassis
17	XBPSD50P08000	AA		C	Screw
⚠ 18	RTRNP1004ACZZ	BQ	N	B	Power transformer
19	XBPBZ40P06K00	AA		C	Screw (4×6K)
20	XBPSD30P06KS0	AA		C	Screw (3×6KS)
21	LANGT1052ACZZ	AG		C	Fan angle
22	XBPSD40P40000	AA		C	Screw (4×40)
23	XWHSD40-08100	AA		C	Washer
24	NFANP1006ACZZ	BG		C	DC Fan
⚠ 100	QCNCM2191SCZZ	AG		B	Connector (3pin)
⚠ 101	QFS-A1002CCZZ	AE		A	Fuse (250V/2A)
⚠ 102	QFSHA1002CCZZ	AB		C	Fuse holder (F-211P)
⚠ 103	RC-CZ1002ACZZ	AD	N	C	Capacitor for lime bypass (2200pF)
⚠ 104	RCiLF1001ACZZ	AH	N	C	Coil
⚠ 105	VCE9HE2EP104K	AK	N	C	Capacitor (250WV 0.1μF)

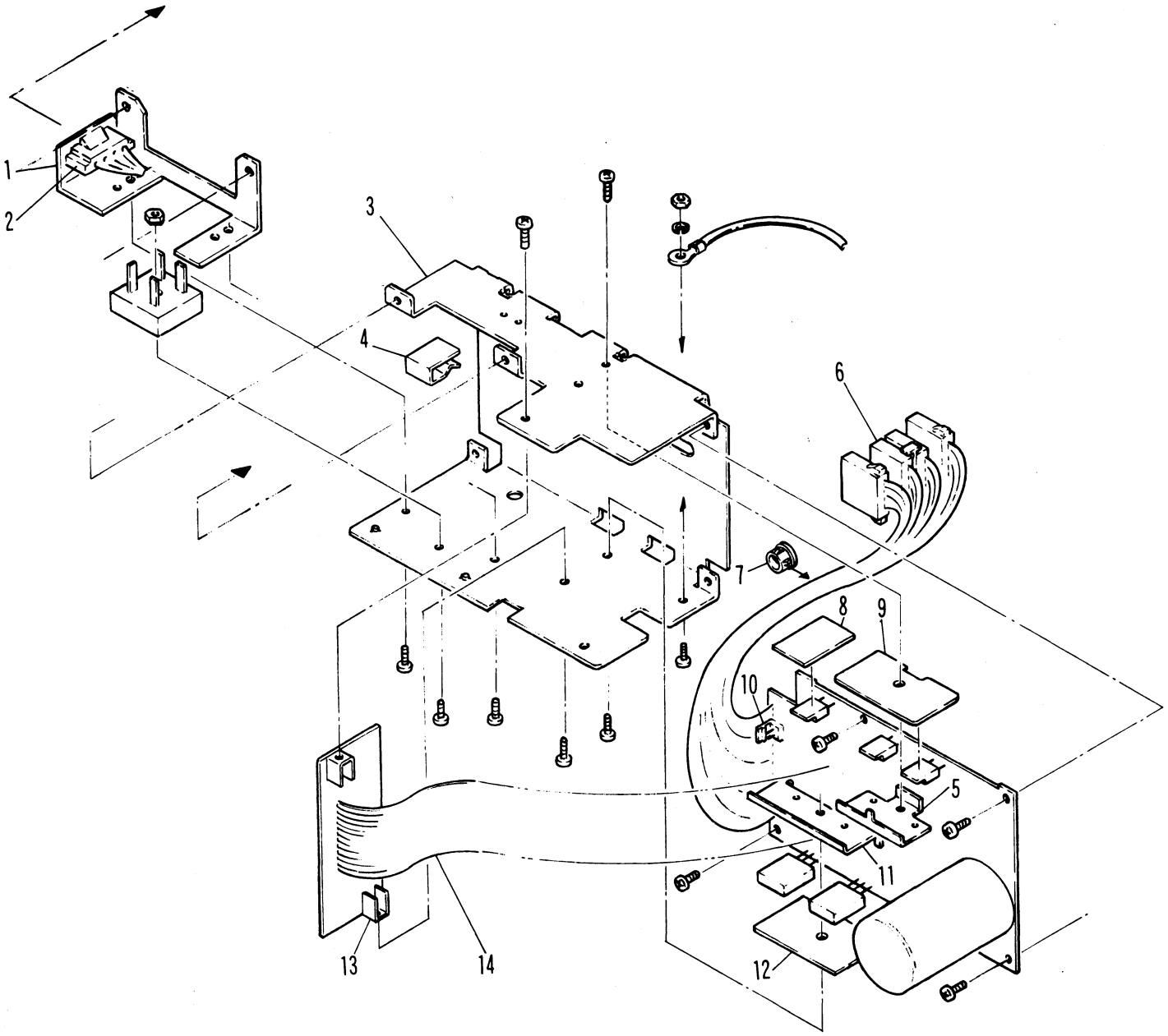


7 Power supply (SEC.) unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	0AE1064648//	AQ	N	C	Angle	
2	0AE1067561//	AT	N	C	Cable (2) for in put (4P)	
3	0AE1064635//	BK	N	C	Chassis	
4	0AE1043908//	AE		C	Clip	
5	0AE1044710//	AE		C	Fixing metal	
6	0AE1067586//	BB	N	C	Cable (1) for out put (4P×2)	
7	0AE2359492//	AC		C	Bushing	
8	0AE1056636//	AC		C	Model label	
9	0AE1044711//	AC		C	Insulator	
10	0AE2066134//	AK	N	C	Connector	
11	0AE1045302//	AD	N	C	Insulator	
12	0AE1048038//	AE		C	Insulator (1)	
13	0AE2360521//	AE	N	C	Terminal	
14	0AE2056838//	AG	N	C	PC Joiner	
50	0AE2066133//	AG	N	C	Band	
51	0AE1045297//	AK	N	C	Holder	
52	0AE1064720//	AK		C	Cable	
101	0AE3027697//	AS	N	B	IC (MB3759M)	[M1,M2]
102	0AE3036204//	AM		B	Transistor (2SC2562−O)	[Q1]
103	0AE3026302//	AD		B	Transistor (2SC1815−Y)	[Q2,Q8,Q9,Q10,Q11]
104	0AE3025878//	AX		B	Transistor (2SC2750−L)	[Q3]
105	0AE3022154//	AG		B	Transistor (2SC2655−Y)	[Q4]
106	0AE3027984//	AK		B	Transistor (2SA1020−Y)	[Q5,Q7,Q12]
107	0AE3024786//	AR	N	B	Transistor (2SC2334−O)	[Q6]
108	0AE3026166//	AD	N	B	Zener diode (HZ12L−31)	[D1]
109	0AE3025885//	AY	N	B	Diode (15SB04M)	[D4]
110	0AE3012194//	AE		B	Diode (1S2348H)	[D5]
111	0AE3026943//	AY		B	Diode (S10SC4M)	[D6]
112	VHD1S2076A/−1	AB		B	Diode (1S2076A−FEC)	[D7,D8]
113	0AE3036208//	AD		B	Zener Diode (HZ7L−C2)	[D9,D10]
114	0AE3050100//	AK		B	Diode (1D4B42)	[RC1]
115	0AE3053043//	BG	N	B	Diode (S25VB10)	[RC2]
116	0AE3020294//	AG		C	Capacitor (50ULB330−M)	[C1]
117	0AE3020069//	AE	N	C	Capacitor (25ULB100−M)	[C2,C18]
118	0AE3052337//	AP		C	Capacitor (KM50VRSN10000HR)	[C3,C22]
119	0AE3012946//	AC		C	Capacitor (50F2S103K)	[C4,C7,C12,C14,C27]
120	0AE3017053//	AC		C	Capacitor (50F2S222K)	[C5]
121	0AE3011999//	AC		C	Capacitor (DD104B471K50V)	[C6,C13]
122	0AE3012052//	AC		C	Capacitor (50F2S223K)	[C8]
123	0AE3022724//	AK		C	Capacitor (10ULB3300−M)	[C9]
124	0AE3016557//	AF		C	Capacitor (10ULB1000−M)	[C10]
125	0AE3014357//	AC		C	Capacitor (50F2S102K)	[C11]
126	0AE3012061//	AD		C	Capacitor (50F2S104K)	[C15,C23,C25]
127	0AE3017000//	AF		C	Capacitor (25ULB330−M)	[C16,C17,C24]
128	0AE3018256//	AD		C	Capacitor (50ULB22−M)	[C19,C21,C28]
129	0AE3016964//	AC	N	C	Capacitor (50ULB4R7−N)	[C20]
130	0AE3012054//	AC		C	Capacitor (50F2S333K)	[C26]
131	0AE3056955//	AC		C	Capacitor (MR25 6.8HM G)	[R1]
132	VRD−ST2EY392J	AA		C	Resistor (CR25 3.9KΩ J F)	[R2]
133	VRD−ST2EY101J	AA		C	Resistor (CR25 100Ω J F)	[R3,R23]
134	0AE3049934//	AC	N	C	Metal oxide resistor (RS1FB 33Ω J)	[R4]
135	VRD−ST2HY151J	AB		C	Resistor (CR37 150Ω J)	[R5,R8]
136	VRD−ST2HY100J	AB	N	C	Resistor (CR37 10Ω J)	[R6]
137	VRD−ST2HY560J	AB	N	C	Resistor (CR37 56Ω J)	[R7]
138	VRS−PT3AB100J	AB	N	C	Metal oxide resistor (RS1FB 10Ω J)	[R9,R28]
139	VRD−ST2EY561J	AA		C	Resistor (CR25 560Ω J F)	[R10]
140	VRD−ST2EY151J	AA		C	Resistor (CR25 150Ω J F)	[R11]
141	VRD−ST2EY123J	AA		C	Resistor (CR25 12KΩ J F)	[R12,R35]
142	VRD−ST2EY153J	AA	N	C	Resistor (CR25 15KΩ J F)	[R13,R29]
143	VRD−ST2EY333J	AA		C	Resistor (CR25 33KΩ J F)	[R14,R45]
144	VRD−ST2EY150J	AA	N	C	Resistor (CR25 15Ω J F)	[R15]
145	VRD−ST2EY562J	AA	N	C	Resistor (CR25 5.6KΩ J F)	[R16,R17,R38]
146	VRD−ST2EY222J	AA		C	Resistor (CR25 2.2KΩ J F)	[R18,R34,R42,R43]
147	VRD−ST2EY472J	AA		C	Resistor (CR25 4.7KΩ J F)	[R19,R20,R32,R33]
148	VRD−ST2EY182J	AA		C	Resistor (CR25 1.8KΩ J F)	[R21]
149	VRD−ST2EY102J	AA		C	Resistor (CR25 1KΩ J F)	[R22,R30,R39,R41,R44,R48]
150	0AE3049132//	AA	N	C	Resistor wire (CNW 1.5 70MM)	[R24]
151	0AE3048125//	AB		C	Metal oxide resistor (1W 22Ω 5%)	[R25]
152	VRD−ST2EY681J	AA		C	Resistor (CR25 680Ω J F)	[R26]
153	0AE3018431//	AB	N	C	Resistor (CR37 4.7KΩ J)	[R27]
154	0AE3024125//	AG	N	C	Cement resistor (MO−4PS 5WV 0.22Ω K)	[R36]
155	VRD−ST2EY511J	AA		C	Resistor (CR25 510Ω J F)	[R37]
156	VRD−ST2EY682J	AA		C	Resistor (CR25 6.8KΩ J F)	[R40]
157	VRD−ST2EY471J	AA		C	Resistor (CR25 470Ω J F)	[R47]
158	0AE3053697//	AG		B	Variable resistor (TM64K (PH) 2KΩ)	[VR1,VR2,VR3]
159	0AE3053696//	AH		B	Variable resistor (TM64K (PH) 500Ω)	[VR4]
⚠ 160	0AE3062445//	AG	N	A	Fuse (014 2A)	[F1]
⚠ 161	0AE3053630//	AW		B	Transformer (TD015)	[T1]
162	0AE3062727//	AX	N	C	Coil (CL15EE270)	[L1]
163	0AE3057437//	AL	N	C	Coil (CL09BE090)	[L2]

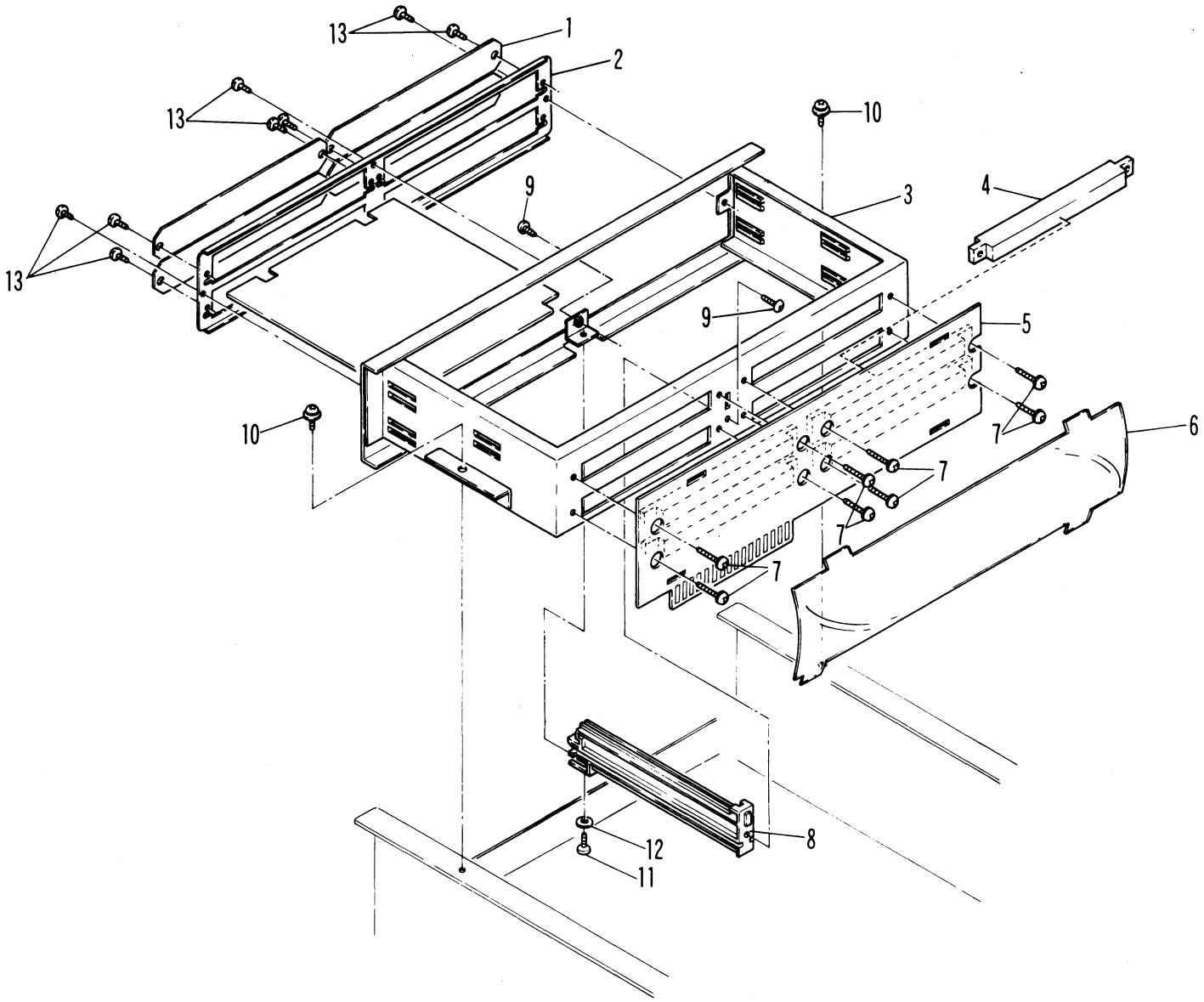
7 Power supply (SEC.) unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
164	0AE3062713 7//	AY	N	C	Coil (CL06EF211) [L3]
165	0AE3057434 5//	AF	N	C	Coil (CL04BD040) [L4]
	(Unit)				
901	DUNT-1316ACZZ	CA	N	E	Power supply (SEC.) unit



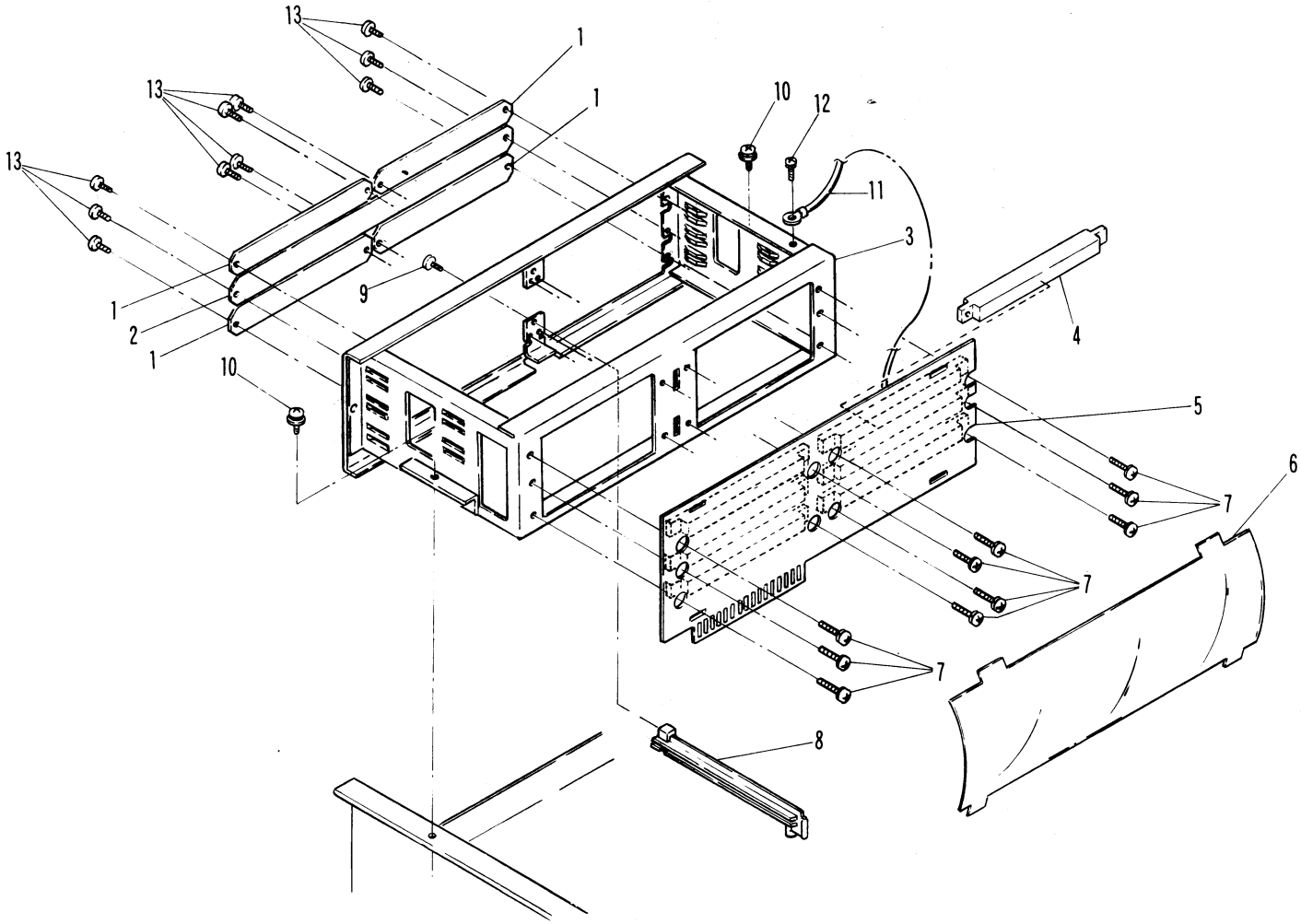
8 Expantion unit For Export (Except Europe)

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	GFTAR1017ACZA	AK		C	Expantion cover
2	GCOVH1005ACZA	AN		C	Expantion cover
3	LCHSM1009ACZZ	AW		D	Expantion box
4	QCNCW1023ACZZ	AT		C	Connector (86pin)
5	DUNTK1197ACZZ	BF		E	Mother board PWB unit (This includes No 4)
6	PZETY1004ACZZ	AE		C	Insulator
7	XBPSD30P10K00	AA		C	Screw (3×10KS)
8	LHLDZ1003ACZZ	AD		C	Guide holder
9	XUPSD30P10000	AA		C	Screw (3×10)
10	XBPSD40P08K00	AA		C	Screw (4×8K)
11	XBPSD30P06000	AA		C	Screw (3×6S/SW)
12	XWHSD30—05080	AA		C	Washer (3HW)
13	XBBSC30P06000	AA		C	Screw (3×6)
	(Unit)				
901	DUNT—1341ACZZ	BU		E	Expantion unit for Ex (Except Europe) (MZ5645) (Ref. block 1—79)



9 Expantion unit For Europe

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	GFTAR1023ACZZ	AF		C	Expantion cover S
2	GFTAR1022ACZZ	AH		C	Expantion cover R
3	LCHSM1015ACZZ	AX		C	Expantion box
4	QCNCW1023ACZZ	AT		C	Connector (86pin)
5	DUNTK1374ACZZ	BU		E	Mother board PWB unit (This includes No 4)
6	PZETY1004ACZZ	AE		C	Insulator
7	XBPSD30P10K00	AA		C	Screw (3×10KS)
8	LHLDZ1007ACZZ	AD		C	Guide plate A
9	XUPSD30P08000	AA		C	Screw (3×8)
10	XBPSD40P08K00	AA		C	Screw (4×8K)
11	QCNW-1082ACZZ	AC		C	Earth wire
12	XBPSD30P06KS0	AA		C	Screw (3×6)
13	XBBSC30P06000	AA		C	Screw (3×6)
101	SPAKC1473ACZZ	AR	N	D	Packing case
102	SSAKA0006UCZZ	AA		D	Vinyl bag (50×60mm)
103	SSAKH0012UCZZ	AB		D	Vinyl bag (450×360mm)
	(Unit)				
901	DUNT-1377ACZZ	BU		E	Expantion unit for Europe only (MZ5645) (Ref. block 1-79)



10 Packing material & Accesaries

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	SPAKA1368ACZZ	BD		D	Packing cushion for set
2	SPAKA1408ACZZ	AY		D	Packing cushion for set (Rear)
3	SPAKC1512ACZZ	AZ	N	D	Packing case (MZ5645)
	SPAKC1511ACZZ	AW	N	D	Packing case (MZ5641)
	SPAKC1510ACZZ	AW	N	D	Packing case (MZ5631)
4	SPAKA5955CCZZ	AC		D	Packing cushion for AC cord
5	SSAKH0004FCZZ	AD		D	Vinyl bag (600×540×510mm)
6	SSAKA0006UCZZ	AA		D	Vinyl bag (50×60mm)
7	PHOG-1023CCZZ	AB		C	Plug (So. Africa)
⚠ 8	QACCB7521QCZZ	AS		B	AC cord (U.Kingdom, So. Africa)
⚠	QACCL7620QCZZ	AW		B	AC cord (Australia only)
⚠	QACCV6620QCZZ	AV		B	AC cord (Other country)
9	QPLGA0018WRE0	AN		C	Plug (So. Africa)
10	UBNDA1008CCZZ	AA		D	Cord band
11	TCAUS1001ACZZ	AB		D	Caution label
12	TLAB-4681CCZZ	AA		C	Ground label (Except So. Africa)
13	QPLGA6626RCZZ	AN		C	Plug (U.Kingdom)

11 D-RAM unit (MZ1R22) For SEEG only (option)

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	MLEVP1001ACZZ	AD		C	PWB Lever
2	RMPTC8102QCKJ	AD		B	Block resistor (1.0KΩ×8 1/16W ±10%)
3	VCEAAU1CW476Q	AB		C	Capacitor (16WV 47μF)
4	VCTYPU1NX104M	AB		C	Capacitor (12WV 0.10μF)
5	VHiCX101///-1	AU		B	IC (CX101)
6	VHiM74LS00/-1	AE		B	IC (M74LS00P)
7	VHiM74LS138-1	AK		B	IC (M74LS138P)
8	VHiM74LS14/-1	AM		B	IC (M74LS14P)
9	VHiM74LS158-1	AG		B	IC (M74LS158P)
10	VHiM74LS20/-1	AE		B	IC (M74LS20P)
11	VHiM74LS245-1	AM		B	IC (M74LS245P)
12	VHiM74LS257-1	AQ		B	IC (M74LS257P)
13	VHiM74LS32/-1	AF		B	IC (M74LS32P)
14	VHi4164-150-H	AZ		B	IC (4164)
15	VRD-ST2EY101J	AA		C	Resistor (1/4W 100Ω ±5%)
16	VRD-ST2EY331J	AA		C	Resistor (1/4W 330Ω ±5%)
17	VRD-ST2EY682J	AA		C	Resistor (1/4W 6.8KΩ ±5%)
18	SPAKA1462ACZZ	AG		D	Packing cushion
19	SPAKC1463ACZZ	AV	N	D	Packing case
20	SPAKA1550ACZZ	AC		D	Packing cushion for protector sheet
21	SSAKH0015HCZZ	AA		D	Vinyl bag (180×280mm)
22	TiNSE1161ACZZ	AS	N	D	Instruction book

12 V-RAM unit (MZ1R09) (option)

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNW-1057ACZZ	AU		C	Lead wire (CRT~V-RAM)
2	VCEAAU1CW336Q	AB		C	Capacitor (16WV 33μF)
3	VCTYPU1NX104M	AB		C	Capacitor (12WV 0.10μF)
4	VHiM74LS244-1	AM		B	IC (M74LS244P)
5	VHiTMS4416-15	AZ	N	B	IC (TMS4416)
6	VRD-ST2EY101J	AA		C	Resistor (1/4W 100Ω ±5%)
7	SPAKA1270ACZZ	AE	N	D	Packing cushion
8	SPAKC1299ACZZ	AT	N	D	Packing case
9	SSAKH1020CCZZ	AA		D	Vinyl bag (120×260mm)
10	TSELF1002ACZZ	AA		D	Label

■ Index

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
【C】					
CCABA1010ACZA	5- 16	AU	N	D	
CCABA1015ACZB	1- 1	BC		D	
CCABA1018ACZA	1- 62	BC	N	D	
CCABB1012ACZA	5- 1	AT	N	D	
CCABC1014ACZB	1- 70	AX		D	
【D】					
DUNT−1182ACZZ	1- 39	**		E	
〃	2- 901	**		E	
DUNT−1316ACZZ	7- 901	CA	N	E	
DUNT−1341ACZZ	1- 79	BU		E	
〃	8- 901	BU		E	
DUNT−1357ACZZ	1- 15	**		E	
DUNT−1377ACZZ	1- 79	BU		E	
〃	9- 901	BU		E	
DUNTK1197ACZZ	8- 5	BF		E	
DUNTK1270ACZZ	1- 81	**		E	
DUNTK1283ACZZ	6- 10	AU		E	
DUNTK1318ACZZ	1- 2	**	N	C	
DUNTK1374ACZZ	9- 5	BU		E	
DUNTK1384ACZZ	4- 901	BV		E	
〃	5- 11	BV		E	
DUNTK1392ACZZ	1- 56	**		E	
〃	3- 901	**		E	
DUNTK1395ACZZ	4- 901	BV		E	
〃	5- 11	BV		E	
【G】					
GCOVH1003ACZZ	5- 3	AD		D	
GCOVH1004ACZZ	5- 2	AC		D	
GCOVH1005ACZA	8- 2	AN		C	
GFTAF1018ACZA	1- 63	AE		D	
GFTAR1017ACZA	8- 1	AK		C	
GFTAR1022ACZZ	9- 2	AH		C	
GFTAR1023ACZZ	9- 1	AF		C	
GFTAU1023ACZZ	1- 57	AM		C	
GLEGP1001CCZZ	5- 14	AB		C	
GLEGP1005ACZZ	1- 64	AB		C	
GSTN−1015ACZA	5- 15	AF	N	C	
【H】					
HBDGB1002ACZZ	1- 72	AD		C	
〃	5- 5	AD		C	
HPNLC1002ACZA	1- 9	AL	N	D	
HPNLC1006ACZZ	6- 15	AE		D	
HPNLC1007ACZZ	6- 4	AN		D	
【J】					
JBTN−1001ACZA	1- 54	AB		C	
JKNBP1006ACZA	1- 71	AD		C	
【L】					
LANGF1069ACZZ	1- 8	AP		C	
LANGT1043ACZZ	1- 25	AL		C	
〃	3- 1	AL		C	
LANGT1051ACZZ	6- 9	AH		C	
LANGT1052ACZZ	6- 21	AG		C	
LANGT1070ACZZ	1- 16	AL		C	
LBNDJ0004UCZZ	1- 14	AA		C	
LBNDJ0009FCZZ	1- 80	AC		D	
LCHSM1009ACZZ	8- 3	AW		D	
LCHSM1014ACZZ	6- 16	AP		C	
LCHSM1015ACZZ	9- 3	AX		C	
LHLDW2334RCZZ	1- 38	AC		C	
LHLDZ1003ACZZ	8- 8	AD		C	
LHLDZ1007ACZZ	9- 8	AD		C	
LSUPP1001ACZZ	1- 45	AB		C	
LSUPP1002ACZZ	1- 42	AC		C	
LSUPP1003ACZZ	1- 27	AB		C	
LX−BZ0038FCZZ	1- 3	AA		C	
LX−BZ1001ACZZ	1- 30	AC		C	
【M】					
MLEVP1001ACZZ	11- 1	AD		C	
【N】					
NFANP1006ACZZ	6- 24	BG		C	
【P】					
PCUSG1006ACZZ	1- 48	AB		C	
PCUSS1002ACZZ	1- 22	AA		C	
PCUSS1008ACZZ	1- 6	AD		C	
PCUSS1011ACZZ	1- 12	AE	N	C	
PHOG−1001ACZZ	1- 49	AC		C	
PHOG−1005ACZZ	1- 65	AC		C	
PHOG−1023CCZZ	10- 7	AB		C	
PSLDM1004ACZZ	5- 17	AM		D	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
PSLDM1005ACZZ	1- 76	AN		C	
PSPAN1007ACZZ	6- 6	AB	N	C	
PZETY1004ACZZ	8- 6	AE		C	
〃	9- 6	AE		C	
【Q】					
QACCB7521QCZZ	10- 8	AS		B	
QACCL7620QCZZ	10- 8	AW		B	
QACCV6620QCZZ	10- 8	AV		B	
QCNCM1009ACZB	1- 51	AA		B	
〃	3- 3	AA		B	
QCNCM1009ACZD	1- 36	AB		C	
〃	2- 1	AB		C	
QCNCM1009ACZE	1- 35	AB		C	
〃	2- 2	AB		C	
QCNCM1009ACZH	1- 26	AC		C	
〃	3- 4	AC		C	
QCNCM1009ACZi	4- 2	AC		C	
〃	5- 8	AC		C	
QCNCM1009ACZJ	3- 5	AC		C	
QCNCM1024ACZZ	1- 43	AP		C	
〃	3- 10	AP		C	
QCNCM1025ACZZ	1- 41	AK		C	
〃	3- 11	AK		C	
QCNCM1026ACZZ	1- 37	AK		C	
〃	2- 3	AK		C	
QCNCM1027ACZZ	1- 34	AP		C	
〃	2- 4	AP		C	
QCNCM1047ACZZ	1- 60	AD		B	
〃	3- 16	AD		B	
QCNCM1048ACZZ	1- 61	AE		B	
〃	3- 17	AE		B	
QCNCM1244CC0B	1- 52	AC		B	
〃	3- 18	AC		B	
QCNCM2191SCZZ	6- 100	AG		B	
QCNCW0207HCZZ	1- 44	AK		C	
〃	3- 2	AK		C	
QCNCW1007ACZZ	4- 1	AE	N	C	
〃	5- 10	AE	N	C	
QCNCW1008AC05	1- 50	AB		B	
QCNCW1017ACZZ	1- 33	AF		C	
〃	3- 6	AF		C	
QCNCW1018ACZZ	4- 3	AF		C	
〃	5- 7	AF		C	
QCNCW1021ACZZ	1- 28	AS		C	
〃	3- 7	AS		C	
QCNCW1022ACZZ	1- 31	AU		C	
〃	3- 8	AU		C	
QCNCW1023ACZZ	1- 29	AT		C	
〃	3- 9	AT		C	
〃	8- 4	AT		C	
〃	9- 4	AT		C	
QCNCW1029ACZZ	1- 32	AU		C	
〃	3- 12	AU		C	
QCNCW1035ACZZ	1- 59	AC		B	
〃	3- 13	AC		B	
QCNCW1040ACZZ	1- 24	AR		C	
〃	3- 14	AR		C	
QCNCW1045ACZZ	1- 23	AP		C	
〃	3- 15	AP		C	
QCNCW1300CC1D	4- 4	AD		C	
〃	5- 9	AD		C	
QCNW−1025AC01	1- 55	AC		C	
QCNW−1052ACZZ	5- 6	AY		C	
QCNW−1053ACZZ	1- 10	AV		C	
QCNW−1054ACZZ	1- 21	AW		C	
QCNW−1055ACZZ	1- 20	AG		C	
〃	2- 5	AG		C	
QCNW−1056ACZZ	1- 10	AZ		C	
QCNW−1057ACZZ	12- 1	AU		C	
QCNW−1072ACZZ	6- 11	AL		C	
QCNW−1077ACZZ	6- 12	AE		C	
QCNW−1078ACZZ	6- 14	AE		C	
QCNW−1082ACZZ	6- 5	AC		C	
〃	9- 11	AC		C	
QCNW−1098ACZZ	1- 77	AS		C	
QCNW−1099ACZZ	1- 78	AV		C	
QFS−A1002CCZZ	6- 101	AE		A	
QFSHA1002CCZZ	6- 102	AB		C	
QJAKC1001ACZZ	1- 53	AD		C	
〃	3- 19	AD		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
QPiN-0019MCZZ	2- 4	AA		C
QPLGA0018WRE0	10- 8	AN		C
QPLGA6626RCZZ	10- 14	AN		C
QPWBE1019ACZZ	1- 60	AB		C
QSOCZ2027SCZZ	6- 7	AK		C
QSOCZ6418ACZZ	3- 20	AD		C
QSOCZ6420ACZZ	3- 21	AB		C
QSOCZ6428ACZZ	3- 22	AC		C
QSOCZ6440ACZZ	3- 23	AC		C
//	4- 5	AC		C
QSW-C9240QCZZ	6- 18	AP		B
QSW-K1025ACZZ	5- 901	BR	N	E
QSW-K1026ACZZ	5- 901	BR	N	E
QSW-K1029ACZZ	5- 901	BR	N	E
QSW-P1022ACZZ	3- 24	AP		B
QSW-Z2002SCZZ	3- 25	AT		B
QTANN1004ACZZ	6- 2	AE	N	C
【R】				
RC-CZ1002ACZZ	6- 101	AB	N	C
RC-KZ1018CCZZ	3- 26	AE		C
RC-KZ1026CCZZ	3- 27	AF		C
RCiLF1001ACZZ	6- 104	AH	N	C
RCiLL1001ACZZ	3- 28	AC		C
RCRS-1004ACZZ	4- 6	AG		B
RCRS-1008ACZZ	2- 7	AT		B
RCRS-1009ACZZ	2- 8	AT		B
RCRS-1016ACZZ	3- 31	AU		B
RCRSP1003CCZZ	3- 29	AT		B
RCRSQ1010ACZZ	3- 30	AK		B
RMPTC4102QCKJ	3- 32	AC		B
RMPTC6331QCKB	3- 33	AC		B
RMPTC8102QCKJ	11- 2	AD		B
RMPTC8224QCMJ	3- 34	AD		B
RMPTC8333QCKJ	4- 7	AD		B
RMPTC8334QCKJ	2- 9	AC		B
RMPTC8682QCKJ	3- 35	AD		B
RTRNP1004ACZZ	6- 18	BQ	N	B
RVR-M1411QCZZ	3- 37	AM		B
RVR-M2411QCZZ	3- 38	AP		B
RVR-Q1001ACZZ	3- 36	AF		B
【S】				
SPAKA1004ACZZ	5- 402	AG	N	D
SPAKA1009ACZZ	5- 403	AB		D
SPAKA1270ACZZ	12- 7	AE	N	D
SPAKA1368ACZZ	10- 1	BD		D
SPAKA1408ACZZ	10- 2	AY		D
SPAKA1413ACZZ	5- 404	AD	N	D
SPAKA1462ACZZ	11- 18	AG		D
SPAKA1550ACZZ	11- 20	AC		D
SPAKA5955CCZZ	10- 4	AC		D
SPAKC1299ACZZ	12- 8	AT	N	D
SPAKC1362ACZZ	5- 405	AL	N	D
SPAKC1364ACZZ	5- 405	AL	N	D
SPAKC1463ACZZ	11- 19	AV	N	D
SPAKC1473ACZZ	9- 101	AR	N	D
SPAKC1510ACZZ	10- 3	AW	N	D
SPAKC1511ACZZ	10- 3	AW	N	D
SPAKC1512ACZZ	10- 3	AZ	N	D
SPAKC1516ACZZ	5- 405	AM	N	D
SSAKA0001SCZZ	5- 406	AA		D
SSAKA0006UCZZ	9- 102	AA		D
//	10- 6	AA		D
SSAKA3630QCZZ	5- 407	AB		D
SSAKH0004FCZZ	10- 5	AD		D
SSAKH0012UCZZ	9- 103	AB		D
SSAKH0015HCZZ	11- 21	AA		D
SSAKH1020CCZZ	12- 9	AA		D
【T】				
TCAUS1001ACZZ	10- 11	AB		D
TiNSE1161ACZZ	11- 22	AS	N	D
TiNSE1175ACZZ	5- 401	BS	N	D
TLAB-4681CCZZ	10- 12	AA		C
TLABZ1029ACZA	5- 4	AB		C
TLABZ1031ACZZ	5- 400	AE		C
TLABZ1035ACZA	1- 17	AB		C
TLABZ1040ACZZ	5- 400	AE		C
TLABZ1050ACZA	1- 13	AB		C
TSELF1002ACZZ	12- 10	AA		D
【U】				
UBATN1001ACZZ	3- 39	AS		A

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
UBNDA1008CCZZ	10- 10	AA		D
【V】				
VCCCPU1HH100D	4- 8	AA		C
VCCCPU1HH120J	3- 40	AA		C
VCCCPU1HH200J	2- 10	AB		C
VCCCPU1HH300J	2- 11	AA		C
VCCCPU1HH470J	3- 41	AA		C
VCCCPU1HH510J	3- 42	AB		C
VCCCPU1HH560J	3- 43	AA		C
VCCCPU1HH820J	3- 44	AB		C
VCEAAU1CW106Q	3- 45	AB		C
VCEAAU1CW107Q	2- 12	AC		C
//	3- 46	AC		C
VCEAAU1CW226Q	3- 47	AB		C
VCEAAU1CW227Q	3- 48	AC		C
VCEAAU1CW336Q	3- 49	AB		C
//	4- 9	AB		C
//	12- 2	AB		C
VCEAAU1CW476Q	11- 3	AB		C
VCEAAU1EW227Q	3- 50	AD		C
VCEAAU1EW336Q	3- 51	AB		C
VCEAAU1EW475Q	4- 10	AB		C
VCEAAU1HW105Q	3- 53	AB		C
VCEAAU1HW225Q	3- 52	AB		C
VCEAAU1HW335Q	3- 54	AB		C
VCE9HE2EP104K	6- 105	AK	N	C
VCKYPU1HB101K	2- 13	AA		C
//	3- 55	AA		C
VCKYPU1HB102K	2- 14	AA		C
//	3- 56	AA		C
VCKYPU1HB121K	3- 57	AA		C
VCKYPU1HB221K	2- 15	AB		C
//	3- 58	AB		C
VCKYPU1HB222K	3- 59	AA		C
VCKYPU1HB561K	3- 60	AA		C
VCKYPU1HB681K	3- 61	AA		C
//	4- 11	AA		C
VCKYPU1HB682K	3- 62	AA		C
VCQSTT2TS271J	3- 63	AD		C
VCQYKU1HM102K	3- 64	AA		C
VCQYKU1HM152K	3- 65	AA		C
VCQYKU1HM333K	3- 66	AB		C
VCQYKU1HM472K	3- 67	AA		C
VCQYKU1HM682K	3- 68	AB		C
VCTYPU1EX472F	3- 129	AA		C
VCTYPU1NX104M	2- 16	AB		C
//	3- 69	AB		C
//	4- 12	AB		C
//	11- 4	AB		C
//	12- 3	AB		C
VHDDS1588L2-1	3- 70	AB		B
//	4- 13	AB		B
VHD1S2075K/-1	5- 150	AB		B
VHD1S2076A/-1	7- 112	AB		B
VHiAY38912/-1	3- 71	AY		B
VHiCX101///-1	3- 72	AU		B
//	11- 5	AU		B
VHiHA16632AP1	3- 73	BH		B
VHiHM6148HL45	3- 74	AV		B
VHiHM6148P/-6	2- 17	AV		B
VHiLH0082A/-1	3- 75	AR		B
VHiLH0084A/-1	3- 76	AW		B
VHiLZ90E07/-1	2- 18	BP	N	B
VHiM74LS00/-1	2- 19	AE		B
//	3- 77	AE		B
//	11- 6	AE		B
VHiM74LS02/-1	3- 78	AE		B
VHiM74LS04/-1	2- 20	AE		B
//	3- 79	AE		B
VHiM74LS05/-1	4- 14	AE		B
VHiM74LS08/-1	2- 21	AE		B
//	3- 80	AE		B
VHiM74LS10/-1	3- 81	AE		B
VHiM74LS11/-1	3- 82	AE		B
VHiM74LS123-1	3- 83	AG		B
VHiM74LS125-1	2- 22	AH		B
//	3- 84	AH		B
VHiM74LS132-1	3- 85	AH		B
VHiM74LS138-1	2- 23	AK		B
//	3- 86	AK		B

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
VHiM74LS138−1	11- 7	AK		B	
VHiM74LS139−1	3- 87	AL		B	
VHiM74LS14/−1	3- 88	AM		B	
〃	4- 15	AM		B	
〃	11- 8	AM		B	
VHiM74LS151−1	3- 89	AK		B	
VHiM74LS157−1	3- 90	AK		B	
VHiM74LS158−1	2- 24	AG		B	
〃	3- 91	AG		B	
〃	11- 9	AG		B	
VHiM74LS163−1	3- 92	AH		B	
VHiM74LS164−1	3- 93	AH		B	
VHiM74LS173−1	3- 94	AG		B	
VHiM74LS174−1	3- 95	AK		B	
VHiM74LS175−1	3- 96	AG		B	
VHiM74LS20/−1	3- 97	AE		B	
〃	11- 10	AE		B	
VHiM74LS244−1	2- 25	AM		B	
〃	12- 4	AM		B	
VHiM74LS245−1	2- 26	AM		B	
〃	3- 99	AM		B	
〃	11- 11	AM		B	
VHiM74LS257−1	3- 100	AQ		B	
〃	11- 12	AQ		B	
VHiM74LS27/−1	3- 101	AF		B	
VHiM74LS30/−1	3- 102	AE		B	
VHiM74LS32/−1	2- 27	AF		B	
〃	3- 103	AF		B	
〃	11- 13	AF		B	
VHiM74LS365−1	3- 104	AF		B	
VHiM74LS367−1	3- 105	AH		B	
VHiM74LS373−1	3- 106	AM		B	
VHiM74LS374−1	2- 28	AM		B	
VHiM74LS393−1	3- 107	AN		B	
VHiM74LS51/−1	2- 29	AE		B	
VHiM74LS670−1	2- 30	AL		B	
VHiM74LS74/−1	2- 31	AG		B	
〃	3- 108	AG		B	
VHiM74LS75/−1	2- 32	AE		B	
VHiM74LS86/−1	3- 109	AF		B	
VHiNE555///−1	3- 110	AG		B	
VHiRP5C01///−1	3- 111	AV		B	
VHiSN74LS00−1	3- 112	AE		B	
VHiSN74LS122N	2- 33	AH		B	
VHiSN74LS166N	2- 34	AN		B	
VHiSN74LS21−1	3- 98	AE		B	
VHiSN74LS257N	2- 35	AG		B	
VHiSN74LS541N	3- 113	AP		B	
VHiSN74S74N−1	2- 36	AF		B	
VHiSN7400N/−1	2- 37	AG		B	
VHiSN7404N/−1	2- 38	AF		B	
〃	3- 114	AF		B	
VHiSN7406N/−1	3- 115	AG		B	
VHiSN7438N/−1	3- 116	AF		B	
VHiSN75188N−1	3- 117	AM		B	
VHiSN75189A−1	3- 118	AP		B	
VHiSP6102C034	2- 39	BA	N	B	
VHiSP6102C035	2- 40	BA	N	B	
VHiTA7313AP−1	3- 119	AL		B	
VHiTC4514BP−1	4- 16	AN		B	
VHiTMS4416−15	2- 41	AZ	N	B	
〃	12- 5	AZ	N	B	
VHiUPD7220D−1	2- 42	BS		B	
VHiUPD765//−1	3- 120	BK		B	
VHiUPD8255/−1	3- 121	AV		B	
VHi2764//AC63	3- 122	BK	N	B	
VHi2764//AC64	3- 122	BK	N	B	
VHi4164−150−H	3- 123	AZ		B	
〃	11- 14	AZ		B	
VHi8086////−2	3- 124	BN		B	
VHi8237A−5M−N	3- 125	BC		B	
VHi8259A///−1	3- 126	AT		B	
VHi8284A///−1	3- 127	AY		B	
VHi8288////−1	3- 128	BG		B	
VHi8749//AC31	4- 17	BS	N	B	
VHPGL9PG2//−1	1- 69	AC		B	
VRD−ST2EY100J	4- 18	AA		C	
VRD−ST2EY101J	2- 44	AA		C	
〃	3- 130	AA		C	
〃	4- 19	AA		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
VRD−ST2EY101J	7- 133	AA		C	
〃	11- 15	AA		C	
〃	12- 6	AA		C	
VRD−ST2EY102J	3- 131	AA		C	
〃	4- 20	AA		C	
〃	7- 149	AA		C	
VRD−ST2EY103J	2- 45	AA		C	
〃	3- 132	AA		C	
VRD−ST2EY104J	3- 133	AA		C	
〃	4- 21	AA		C	
VRD−ST2EY121J	1- 67	AA		C	
〃	4- 22	AA		C	
VRD−ST2EY122J	3- 134	AA		C	
VRD−ST2EY123J	3- 161	AA		C	
〃	7- 141	AA		C	
VRD−ST2EY150J	7- 144	AA	N	C	
VRD−ST2EY151J	7- 140	AA		C	
VRD−ST2EY153J	7- 142	AA	N	C	
VRD−ST2EY182J	7- 148	AA		C	
VRD−ST2EY183J	3- 145	AA		C	
VRD−ST2EY220J	2- 46	AA		C	
VRD−ST2EY221J	3- 135	AA		C	
VRD−ST2EY222J	4- 23	AA		C	
〃	7- 146	AA		C	
VRD−ST2EY223J	3- 136	AA		C	
VRD−ST2EY331J	3- 137	AA		C	
〃	11- 16	AA		C	
VRD−ST2EY332J	3- 138	AA		C	
VRD−ST2EY333J	3- 139	AA		C	
〃	4- 24	AA		C	
〃	7- 143	AA		C	
VRD−ST2EY334J	2- 47	AA		C	
VRD−ST2EY392J	3- 140	AA		C	
〃	7- 132	AA		C	
VRD−ST2EY471J	3- 141	AA		C	
〃	7- 157	AA		C	
VRD−ST2EY472J	3- 142	AA		C	
〃	4- 25	AA		C	
〃	7- 147	AA		C	
VRD−ST2EY473J	3- 143	AA		C	
VRD−ST2EY511J	7- 155	AA		C	
VRD−ST2EY561J	3- 144	AA		C	
〃	7- 139	AA		C	
VRD−ST2EY562J	7- 145	AA	N	C	
VRD−ST2EY563J	3- 146	AA		C	
VRD−ST2EY681J	4- 26	AA		C	
〃	7- 152	AA		C	
VRD−ST2EY682J	3- 147	AA		C	
〃	4- 27	AA		C	
〃	7- 156	AA		C	
〃	11- 17	AA		C	
VRD−ST2HY100J	7- 136	AB	N	C	
VRD−ST2HY151J	7- 135	AB		C	
VRD−ST2HY560J	7- 137	AB	N	C	
VRD−SU2EY101J	2- 48	AA		C	
VRD−SU2EY121J	3- 148	AA		C	
VRD−SU2EY152J	3- 149	AA		C	
VRD−SU2EY224J	3- 150	AA		C	
VRD−SU2EY241J	3- 151	AA		C	
VRD−SU2EY331J	2- 49	AA		C	
VRD−SU2EY391J	3- 152	AA		C	
VRD−SU2EY470J	3- 153	AA		C	
VRD−SU2EY511J	3- 154	AA		C	
VRD−SU2EY560J	3- 155	AA		C	
VRD−SU2EY680J	3- 156	AA		C	
VRD−SU2EY681J	3- 157	AA		C	
VRD−SU2EY750J	3- 158	AA		C	
VRD−SU2EY821J	3- 159	AA		C	
VRD−SU2EY824J	3- 160	AA		C	
VRN−RT2EK153F	3- 162	AB		C	
VRN−RT2EK203F	3- 163	AB		C	
VRN−RT2EK513F	3- 164	AB		C	
VRS−PT3AB100J	7- 138	AB	N	C	
VSP0080P−608N	1- 47	AN		B	
VS2SA673−D/−1	3- 165	AC		B	
VS2SA733−//−1	3- 166	AD		B	
VS2SC1317−S−1	3- 167	AC		B	
VS2SC641KC/−1	3- 168	AE		B	
VS2SC945///−1	3- 169	AD		B	
〃	4- 28	AD		B	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
VS2SK168−//−1	3- 170	AD		B
〔X〕				
XBBSC30P06000	8- 13	AA		C
//	9- 13	AA		C
XBBSC30P08000	1- 4	AA		C
XBBSD30P06000	6- 8	AA		C
XBPBZ40P06K00	6- 19	AA		C
XBPSD30P04000	5- 117	AA		C
XBPSD30P05000	1- 74	AA		C
//	6- 1	AA		C
XBPSD30P06KS0	1- 19	AA		C
//	6- 20	AA		C
//	9- 12	AA		C
XBPSD30P06000	8- 11	AA		C
XBPSD30P08K00	1- 11	AA		C
//	1- 18	AA		C
XBPSD30P10K00	8- 7	AA		C
//	9- 7	AA		C
XBPSD40P05K00	1- 11	AA		C
XBPSD40P08K00	1- 7	AA		C
//	8- 10	AA		C
//	9- 10	AA		C
XBPSD40P10KS0	1- 46	AA		C
XBPSD40P40000	6- 22	AA		C
XBPSD50P08000	6- 17	AA		C
XBPSM30P04K00	3- 171	AA		C
XBPSM30P06KS0	5- 12	AA		C
XBPSM30P10K00	3- 172	AA		C
XBSSD30P06000	1- 75	AA		C
XBTSC40P06000	1- 73	AA		C
XCPSD40P12000	1- 58	AA		C
XUPSC30P10000	5- 13	AA		C
XUPSD30P06000	1- 66	AA		C
XUPSD30P08000	9- 9	AA		C
XUPSD30P10000	8- 9	AA		C
XWHNZ30−05080	1- 5	AA		C
XWHSD30−05080	8- 12	AA		C
XWHSD40−08100	6- 23	AA		C
〔0〕				
0AE10432908//	7- 4	AE		C
0AE10447100//	7- 5	AE		C
0AE10447113//	7- 9	AC		C
0AE10452973//	7- 51	AK	N	C
0AE10453026//	7- 11	AD	N	C
0AE10480387//	7- 12	AE		C
0AE10566366//	7- 8	AC		C
0AE10646435//	7- 3	BK	N	C
0AE10646448//	7- 1	AQ	N	C
0AE10647201//	7- 52	AK		C
0AE10675613//	7- 2	AT	N	C
0AE10675862//	7- 6	BB	N	C
0AE20568380//	7- 14	AG	N	C
0AE20661339//	7- 50	AG	N	C
0AE20661342//	7- 10	AK	N	C
0AE23594924//	7- 7	AC		C
0AE23605211//	7- 13	AE	N	C
0AE30119991//	7- 121	AC		C
0AE30120524//	7- 122	AC		C
0AE30120540//	7- 130	AC		C
0AE30120618//	7- 126	AD		C
0AE30121947//	7- 110	AE		B
0AE30129460//	7- 119	AC		C
0AE30143572//	7- 125	AC		C
0AE30165576//	7- 124	AF		C
0AE30169640//	7- 129	AC	N	C
0AE30170008//	7- 127	AF		C
0AE30170532//	7- 120	AC		C
0AE30182562//	7- 128	AD		C
0AE30184311//	7- 153	AB	N	C
0AE30200693//	7- 117	AE	N	C
0AE30202947//	7- 116	AG		C
0AE30221546//	7- 105	AG		B
0AE30227249//	7- 123	AK		C
0AE30241254//	7- 154	AG	N	C
0AE30247863//	7- 107	AR	N	B
0AE30258784//	7- 104	AX		B
0AE30258852//	7- 109	AY	N	B
0AE30261661//	7- 108	AD	N	B
0AE30263025//	7- 103	AD		B
0AE30269430//	7- 111	AY		B

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
0AE30276973//	7- 101	AS	N	B
0AE30279844//	7- 106	AK		B
0AE30362049//	7- 102	AM		B
0AE30362081//	7- 113	AD		B
0AE30481250//	7- 151	AB		C
0AE30491321//	7- 150	AA	N	C
0AE30499349//	7- 134	AC	N	C
0AE30501004//	7- 114	AK		B
0AE30523370//	7- 118	AP		C
0AE30530431//	7- 115	BG	N	B
0AE30536309//	7- 161	AW		B
0AE30536969//	7- 159	AH		B
0AE30536972//	7- 158	AG		B
0AE30569554//	7- 131	AC		C
0AE30574345//	7- 165	AF	N	C
0AE30574374//	7- 163	AL	N	C
0AE30624457//	7- 160	AG	N	A
0AE30627137//	7- 164	AY	N	C
0AE30627276//	7- 162	AX	N	C
00PC5KC083001	5- 201	AK	N	C
00PC5KC083002	5- 202	AK	N	C
00PC5KC083003	5- 203	AK	N	C
00PC5KC083004	5- 204	AK	N	C
00PC5KC083005	5- 205	AK	N	C
00PC5KC083006	5- 206	AK	N	C
00PC5KC083007	5- 207	AK	N	C
00PC5KC083008	5- 208	AK	N	C
00PC5KC083009	5- 209	AK	N	C
00PC5KC083010	5- 210	AK	N	C
00PC5KC083011	5- 211	AK	N	C
00PC5KC083012	5- 272	AK	N	C
00PC5KC083013	5- 273	AK	N	C
00PD2KC009001	5- 242	AQ	N	C
00PD2KC009002	5- 269	AQ	N	C
00PKB34884D//	5- 271	AK	N	C
00PKCL10004−Z	5- 103	AH		B
00PKCL10901−Z	5- 102	AH		B
00PKCL10903−Z	5- 101	AH		B
00PKCL11901−Z	5- 116	AP	N	B
00PKCL11902−Z	5- 116	AL	N	B
00P08KC275B//	5- 104	BK	N	C
00P08KC392A//	5- 104	BK	N	C
00P13KF015A//	5- 124	AB		C
00P16KC004A//	5- 105	AG		C
00P16KF006A//	5- 106	AG		C
00P19KC003A//	5- 107	AE		C
00P21KC005A//	5- 110	AK		C
00P21KC006A//	5- 109	AN		C
00P21KC007A//	5- 111	AN		C
00P21KC008A//	5- 126	AK	N	C
00P21KC013A//	5- 108	AE		C
00P23KF001A//	5- 122	AC		C
00P24KC015N//	5- 125	AD		C
00P24KC027A//	5- 113	AK		C
00P24KC032A//	5- 112	AN		C
00P25KF008A//	5- 123	AC		C
00P29KC049A//	5- 121	AK		C
00P29KF006B//	5- 120	AK		C
00P4D07177A//	5- 115	AK	N	B
00P80L7C52000	5- 270	AQ		C
00P80M2C41001	5- 267	AQ	N	C
00P80M4C41001	5- 240	AQ	N	C
00P81T7C41001	5- 278	AQ	N	C
00P81T8C41002	5- 267	AQ	N	C
00P81T9C41001	5- 281	AQ	N	C
00P81U5C41001	5- 301	AQ	N	C
00P81V3C41001	5- 226	AQ	N	C
00P82F5C41001	5- 227	AQ	N	C
00P83L8C41001	5- 255	AQ	N	C
00P84E1C41001	5- 212	AQ	N	C
00P86N1C41001	5- 274	AK	N	C
00P86N1C41002	5- 275	AK	N	C
00P86N1C41003	5- 286	AK	N	C
00P86N1C41004	5- 287	AK	N	C
00P86N1C41005	5- 288	AK	N	C
00P86N1C41006	5- 289	AK	N	C
00P86N1C52001	5- 213	AK	N	C
00P86N1C52004	5- 216	AK	N	C
00P86N1C52005	5- 217	AK	N	C
00P86N1C52011	5- 224	AK	N	C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
00P86N1C52014	5- 214	AK	N	C	
00P86N1C52015	5- 218	AK	N	C	
00P86N1C52016	5- 219	AK	N	C	
00P86N1C52017	5- 220	AK	N	C	
00P86N1C52018	5- 221	AK	N	C	
00P86N1C52019	5- 222	AK	N	C	
00P86N1C52020	5- 223	AK	N	C	
00P86N1C52021	5- 224	AK	N	C	
00P86N1C52023	5- 215	AK	N	C	
00P86N1C52024	5- 219	AK	N	C	
00P86N1C52025	5- 222	AK	N	C	
00P86N1C52026	5- 223	AK	N	C	
00P86N1C52027	5- 224	AK	N	C	
00P86N1C52028	5- 225	AK	N	C	
00P86N1C52044	5- 213	AK	N	C	
00P86N1C52045	5- 214	AK	N	C	
00P86N1C52046	5- 215	AK	N	C	
00P86N1C52047	5- 216	AK	N	C	
00P86N1C52048	5- 217	AK	N	C	
00P86N1C52049	5- 218	AK	N	C	
00P86N1C52050	5- 219	AK	N	C	
00P86N1C52051	5- 220	AK	N	C	
00P86N1C52053	5- 222	AK	N	C	
00P86N1C52054	5- 223	AK	N	C	
00P86N1C52074	5- 215	AK	N	C	
00P86N1C52078	5- 221	AK	N	C	
00P86N2C41001	5- 276	AK	N	C	
00P86N2C41002	5- 277	AK	N	C	
00P86N2C41003	5- 293	AK	N	C	
00P86N2C52001	5- 228	AK	N	C	
00P86N2C52002	5- 229	AK	N	C	
00P86N2C52003	5- 230	AK	N	C	
00P86N2C52004	5- 231	AK	N	C	
00P86N2C52005	5- 232	AK	N	C	
00P86N2C52006	5- 233	AK	N	C	
00P86N2C52007	5- 234	AK	N	C	
00P86N2C52008	5- 235	AK	N	C	
00P86N2C52009	5- 236	AK	N	C	
00P86N2C52010	5- 237	AK	N	C	
00P86N2C52011	5- 239	AK	N	C	
00P86N2C52013	5- 290	AK	N	C	
00P86N2C52014	5- 291	AK	N	C	
00P86N2C52015	5- 292	AK	N	C	
00P86N2C52016	5- 238	AK	N	C	
00P86N2C52017	5- 229	AK	N	C	
//	5- 233	AK	N	C	
00P86N2C52018	5- 238	AK	N	C	
00P86N2C52019	5- 239	AK	N	C	
00P86N2C52020	5- 228	AK	N	C	
00P86N2C52026	5- 238	AK	N	C	
00P86N2C52027	5- 239	AK	N	C	
00P86N3C41096	5- 241	AK	N	C	
00P86N3C41097	5- 297	AK	N	C	
00P86N3C52001	5- 243	AK	N	C	
00P86N3C52002	5- 244	AK	N	C	
00P86N3C52003	5- 245	AK	N	C	
00P86N3C52004	5- 246	AK	N	C	
00P86N3C52005	5- 247	AK	N	C	
00P86N3C52006	5- 248	AK	N	C	
00P86N3C52007	5- 249	AK	N	C	
00P86N3C52008	5- 250	AK	N	C	
00P86N3C52009	5- 251	AK	N	C	
00P86N3C52013	5- 294	AK	N	C	
00P86N3C52014	5- 296	AK	N	C	
00P86N3C52015	5- 252	AK	N	C	
00P86N3C52016	5- 253	AK	N	C	
00P86N3C52017	5- 254	AK	N	C	
00P86N3C52018	5- 252	AK	N	C	
00P86N3C52019	5- 253	AK	N	C	
00P86N3C52020	5- 254	AK	N	C	
00P86N3C52021	5- 243	AK	N	C	
00P86N3C52022	5- 252	AK	N	C	
00P86N3C52047	5- 254	AK	N	C	
00P86N3C52048	5- 253	AK	N	C	
00P86N4C41001	5- 279	AK	N	C	
00P86N4C41002	5- 280	AK	N	C	
00P86N4C52001	5- 256	AK	N	C	
00P86N4C52002	5- 257	AK	N	C	
00P86N4C52003	5- 258	AK	N	C	
00P86N4C52004	5- 259	AK	N	C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
00P86N4C52005	5- 260	AK	N	C	
00P86N4C52006	5- 261	AK	N	C	
00P86N4C52007	5- 262	AK	N	C	
00P86N4C52008	5- 263	AK	N	C	
00P86N4C52009	5- 264	AK	N	C	
00P86N4C52010	5- 265	AK	N	C	
00P86N4C52011	5- 298	AK	N	C	
00P86N4C52012	5- 299	AK	N	C	
00P86N4C52013	5- 300	AK	N	C	
00P86N4C52014	5- 266	AK	N	C	
00P86N4C52015	5- 256	AK	N	C	
00P86N4C52016	5- 263	AK	N	C	
00P86N4C52017	5- 264	AK	N	C	
00P86N4C52018	5- 265	AK	N	C	
00P86N4C52020	5- 256	AK	N	C	
00P86N4C52041	5- 262	AK	N	C	
00P86N4C52042	5- 263	AK	N	C	
00P86N4C52043	5- 264	AK	N	C	
00P86N4C52044	5- 265	AK	N	C	
00P86N4C52061	5- 225	AK	N	C	
00P86N5C41001	5- 268	AK	N	C	
00P86N5C41002	5- 271	AK	N	C	
00P86N5C52001	5- 302	AK	N	C	
00P86N5C52002	5- 303	AK	N	C	
00P86N5C52003	5- 304	AK	N	C	
00P86P6C52001	5- 295	AK	N	C	
00P86P7C41000	5- 282	AK	N	C	
//	5- 283	AK	N	C	
//	5- 284	AK	N	C	
//	5- 285	AK	N	C	

SHARP

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